CCD Data Acquisition Systems at Lick and Keck Observatories

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Abstract. This paper describes the evolution of the existing CCD Data Acquisition System (DAS) at Lick Observatory, and its influence on the design of the CCD DAS currently under development for Keck Observatory. Tradeoffs between various types of interfaces between instrument computers and CCD controllers are also explored.

1. Introduction

Before discussing the design of CCD Data Acquisition Systems (DAS), it is useful to briefly review the major functions they perform. We omit those DAS functions which are instrument or telescope-specific and not directly tied to the operation of the CCD.

1.1. Dewar and chip-level functions

These include: generation of CCD clocking waveforms and bias voltages, signal processing and digitization of the video signal(s) from the CCD, transmission of the digitized data, exposure timing and shutter control, dewar temperature sensing and control, and optionally, dewar cryogen level sensing and control.

1.2. Image recording functions

These include: collecting (and, if needed, descrambling) the pixel data stream from the CCD, collecting all relevant observational parameters (e.g., exposure time, image dimension) for the FITS header, and recording the header and pixel data to disk and/or tape. Sufficient parameters should be recorded to allow subsequent data reduction and analysis. Additional parameters should be recorded to accurately describe all controllable aspects (e.g., CCD, instrument, and telescope) of an exposure so that a nearly-identical one can be recreated at a later time (Conrad 1992). Ideally, the complete image file, or at least its FITS header, should be automatically entered into an archival data base.

1.3. Image Display Functions

These include both the real-time display of CCD images as they are being read out, and the display of previously recorded images. Such displays should at least provide adjustable intensity mapping and modes (e.g., linear, log), panning and zooming, interactive cursor readout, row and column plots of selected regions, and basic image statistics (e.g., image centroids, FWHM).

1.4. User interface functions

These include status display and control of: exposure state, time, and type (e.g., dark frame); CCD binning and windowing; readout modes (e.g., MPP); number and configuration of readout amplifiers; current image file directory and file name; frame number; recording modes (e.g., disk/tape); dewar temperature and cryogen level.

The user interface functions should be isolated into a separate series of processes, and loosely-coupled to the underlying hardware control processes by a well-defined interface protocol. This permits such user interfaces to be shared across multiple instruments (Lupton 1992 and Conrad 1992).

1.5. Engineering functions

These include: real-time modification and display of CCD waveforms and bias voltages, system performance measurements (e.g., readout noise), and subsystem diagnostics (e.g., data link loopback testing, power supply monitoring). For safety of the CCD, such functions would be inaccessible during routine observing, and would be reserved for qualified engineering and technical support personnel.

2. Evolution of the existing CCD DAS at Lick Observatory

The first incarnation of the Lick CCD DAS was implemented in 1980. It established a basic model for the partitioning of CCD DAS functions which has endured for nearly 12 years. This model consists of 2 major hardware components: a CCD controller, located in close proximity to the CCD dewar, which performs the dewar/chip-level functions, and an instrument computer, remotely located in the control room, which performs the remaining CCD DAS functions. These two components are linked by the Lick serial multiplexer bus, a custom serial link developed at Lick during the early 1970s and which until recently formed the main communications and control network at the Lick telescopes. The custom hardware and associated software device drivers required to operate this link were embedded directly into both the CCD controller and the instrument computer, both for efficiency and economy.

2.1. PDP-8/I system, 1980-1981

In the initial 1980 version, the instrument computer was a DEC PDP-8/I minicomputer (a 1970s vintage machine acquired for running the Lick IDS scanner), with 32K 12-bit words of physical memory plus floppy disk and 9-track magnetic tape (Lauer 1981). The 12-bit word size was well matched to the fast 12-bit analog to digital converters (ADCs) of that era. The CCD controller (custom built at Lick) employed a Rockwell 6502 8-bit microprocessor, was programmed in assembly language, and utilized 2KB UV-erasable EPROM chips for program and waveform table storage (Robinson 1987). This overall system was barely adequate during our first few years of CCD observing, and was quickly overwhelmed as CCD dimensions and ADC resolutions increased.

2.2. LSI-11 systems, 1982-1987

In 1982, the PDP-8/I instrument computer was replaced by DEC LSI-11/23 and LSI-11/73 Qbus-based systems, programmed in C and running a derivative of Bell Labs Version 7 Unix. The instrument computer side of the CCD DAS was re-written by Stover to utilize the multi-tasking capabilities of Unix, and the user interface functions were split off into a separate process which communicated with the underlying hardware-control processes by means of pipes. The custom PDP-8-based hardware and software drivers for the Lick serial multiplexer had to be re-designed and re-implemented for the LSI-11/Q-bus/Unix system. The CCD controller remained much the same, except that the 12-bit ADC was replaced with a 15-bit device to take advantage of the increased word size provided by the LSI-11 systems.

2.3. ISI 680x0 systems, 1987-present

Once again, advances in both CCD and computer technology overtook the capabilities of the instrument computer, and the LSI-11s were replaced with Integrated Solutions (ISI) computers in 1987. These ISI systems initially contained dual Motorola 68020-series CPUs (upgraded to 68030 CPUs in 1989) sharing a common VME-bus backplane. The first CPU is master of most of the peripherals such as disks, tapes, and image displays, and runs the non-time-critical user interface, data display, and data reduction processes. The second CPU, which is diskless, is dedicated to real-time control of the lower-level hardware, including processes for operating the CCD controller, the instrument controller, and the telescope controller. The two CPUs communicate via shared VME-bus memory, via sockets over the backplane, and via ISI's transparent remote file system which allows access to the disk from the second CPU.

Most of the C code from the LSI-11-based DAS ported directly to the ISI systems, which run a derivative of Berkeley 4.3 Unix. The separate user interface was retained in much the same form, but pipes were replaced by sockets. The MUSIC system was created (Stover 1989), which introduced three additional DAS processes (traffic, infoman, and runner) to coordinate distributed processing between the two CPUs and to provide for multiple instances of the user interface process. This latter feature made possible coordinated local/remote observing. Yet again, the custom hardware and software drivers for the Lick serial multiplexer were re-implemented to accommodate the change from the Qbus to the VME-bus and from Bell to Berkeley Unix. During this transition, the CCD controller remained virtually unchanged.

The ISI-based systems are still the primary ones used both at the Lick telescopes on Mount Hamilton and at the Lick CCD Detector Development laboratory on the UC Santa Cruz campus. The important trend to note in this 12-year evolution is that while the instrument computer side of the model has gone through multiple changes of processor architecture, hardware bus, and operating system, the CCD controller side has remained virtually unchanged. Also note that a non-negligible portion of the cost and delay associated with each instrument computer upgrade was the re-design and re-implementation of the custom hardware and device drivers required to support the embedded interface to the CCD controller.

2.4. New architectural model, SPARC system, 1992

In mid-1992, Stover implemented a CCD DAS at Lick which represents the first significant departure from the two-component 'instrument computer/CCD controller' model. In this new system (developed for the Coudé Auxiliary Telescope attached to the Shane 3-meter Telescope at Lick), a Sun Sparcstation (which has no VME-bus) is used as the instrument computer. However, rather than attempting to redesign the custom hardware for the Lick multiplexer (in this case, to work with the Sparc's S-bus) and embed it within the instrument computer, the custom hardware (and software) instead was isolated to a separate, diskless, VME-bus chassis. The Sparc instrument computer thus remains a standard 'off-the-shelf' system, containing no custom hardware or device drivers.

The separate VME-bus chassis (which we refer to as the data capture computer) represents a third component of the model, and logically sits between the instrument computer and the CCD controller. It contains basically the same VME-bus hardware as used on the ISI systems for interfacing to the Lick multiplexer. It also contains a Sparc-1E processor board, running SunOS 4.1e, which assumes most of the functions previously performed by the second CPU in the ISI systems. The Sparc-1E board boots from the Sparc instrument computer via Ethernet, and the custom device driver required to operate the Lick multiplexer is emulated on the Sparc-1E using the Unix mmap() system function. The data capture computer receives the pixel stream from the CCD controller, combines this data with appropriate FITS header data, and records, via NFS, the resulting image file on a remotely-mounted disk partition of the instrument computer. By isolating the custom hardware and software into the data capture computer, and using only a well-accepted industry standard interface to connect it to the instrument computer, future upgrades and/or replacement of the instrument computer hardware and software should be greatly simplified.

3. The Keck Observatory CCD DAS

An overview of the hardware architecture for the Keck CCD DAS show 3 major components: an 'off-the-shelf' instrument computer, a semi-custom data capture computer, and a CCD controller. At this level, the architecture is quite similar to that of the recently-implemented system at Lick described in the previous section. The similarity extends to a lower level, in that the Keck system (at least currently) employs a Sparc-based instrument computer, and a Sparc-1E-based VME-bus crate for the data capture computer. There, however, the similarity ends, since the Keck CCD DAS utilizes a completely different CCD controller, which connects to the data capture computer through an entirely new interface.

3.1. The Leach CCD controller

Although the existing Lick CCD controller has proved to be a reliable workhorse over the past decade, it is clearly obsolete and does not provide all the features desired for the Keck system, such as dynamically programmable CCD waveforms or support for large numbers of readout amplifiers. Although some consideration was initially given to developing a completely new CCD controller, the system developed by Bob Leach at San Diego State University was found to meet the requirements for the Keck system (Leach 1990).

The Leach system is based on Motorola DSP56001 digital signal processors (DSPs) which are highly-parallel processors capable of performing multiple simultaneous functions at a 10 MHz rate. These processors are programmed in DSP assembler, and the software and CCD waveform tables are stored in an onboard EEROM which can either be programmed off-line in a PROM burner, or in-place at runtime via a 40 MHz dual-fiber optic link which connects the Leach CCD controller to the data capture computer. The Leach CCD controller provides all of the dewar and chip-level functions, and supports interleaved readout from large numbers (16 or more) of amplifiers.

The Leach controller is gaining fairly wide acceptance, and is currently in use at San Diego State University (SDSU), UCO/Lick Observatory, Caltech, Michigan Dartmouth MIT Observatory (MDM), University of Chicago, Universitie de Paris-Meudon, and Steward Observatory. It is also becoming somewhat of a standard on Mauna Kea, where it is also used at the Canada-France-Hawaii Telescope (CFHT), University of Hawaii Institute for Astronomy (UH-IfA), and Keck Observatory.

3.2. Interfacing to the Leach CCD controller

The 40 MHz fiber optic link from the Leach CCD controller represents much the same problem as the 4 MHz serial multiplexer link from the existing Lick CCD controllers. Since both are non-standard, they require some sort of custom hardware and software interface. Unfortunately, while the Leach CCD controllers are becoming somewhat of a standard, most institutions have developed their own unique interface. Many of these interfaces were developed in parallel, and some of these are described in detail elsewhere in these proceedings.

In the UH-IfA system (Jim 1992), the Leach CCD controller is interfaced via a small, external, custom fiber-optic adapter card to a DSP-input port on a NeXT computer, which contains an integral DSP56001 as standard equipment. The NeXT serves as the data capture computer and also provides an excellent software development environment for the DSP-software for the Leach controllers. The NeXT also replicates some of the functionality of the instrument computer, although images can also be uploaded via Ethernet to a SPARC-2 host for more extensive processing. The UH-IfA system is relatively inexpensive, efficient, and compact.

In the MDM system (Metzger 1992), the Leach CCD controller is interfaced to a Sun SPARC-2 via an external custom hardware interface which connects to a DR-11W parallel interface emulator attached to the Sparc's internal S-bus. In this case, the SPARC-2 may be viewed as the instrument computer with an embedded custom interface to the CCD controller, as was the case under the original Lick 2-component CCD DAS model. This system involves minimal hardware, and is also quite inexpensive and compact. Since the pixel data stream is transferred directly from the CCD controller to the SPARC-2, any potential Ethernet bandwidth limitations are avoided.

Other permutations exist, involving possible combinations of the above two systems using a DSP56001 S-bus board manufactured by Ariel. In addition, Leach has recently released his own custom-designed VME-bus DMA controller board, which employs an on-board DSP56001 both to implement the VME-bus DMA-handshaking as well as to provide the interface to the fiber optic link from the Leach CCD controller.

More recently, a proposal to the Keck project has been advanced by McCarthy at Caltech and Stubbs at UCSB to design a SCSI-based interface to the Leach CCD controller. This proposed interface would emulate a SCSI device on the instrument computer side, and provide an internal memory buffer and fiber optic interface on the Leach CCD controller side. Since SCSI is a widely-accepted industry standard, such an interface could greatly simplify the task of interfacing the Leach controllers to a variety of both new and existing computer equipment.

Since none of these systems existed at the time that the Keck CCD DAS was specified, it employs yet another flavor of interface to the Leach CCD controller. As mentioned earlier, the data capture computer in the Keck system consists of a VME-bus crate containing a SPARC-1E board connected to the instrument computer via Ethernet. The VME-bus crate also contains a 32MB VME-bus memory board, for local buffering of complete CCD images, and an IKON DR11-W (emulator) parallel interface DMA controller board, which transfers the pixel data stream into the VME-bus memory via DMA. All of this is 'off-the-shelf' hardware. The IKON DR11-W board in turn connects (via two DR11-W-style ribbon cables) to a custom-built wire-wrapped board which provides the interface to the the fiber optic link from the Leach CCD controller.

This custom interface board can buffer 4K pixels of data in an on-board FIFO, and provides dual pathways to the VME-bus memory. Data can be transferred between the board and the VME-bus memory under DMA control via the IKON board, or directly via the VME-bus, using programmed I/O from the SPARC-1E. Extensive internal and external hardware loopback modes are provided to facilitate maintenance of this custom board.

During CCD readout, pixels are received by the data capture computer via the fiber link from the Leach CCD controller and transferred (via DMA) into the VME-bus memory. As each successive group of pixels (typically several thousand pixels) is received, it is packaged into UDP-datagrams by vxWorks-based software running on the Sparc-1E, and sent via Ethernet to the instrument computer, using a reliable, high-performance image-transmission protocol. There the image data are received, displayed in real-time, combined with FITS header data, and recorded. As soon as the last pixel of an image has been read out, sent down the fiber, and transferred via DMA into the VME-bus memory on the data capture computer, the next exposure can immediately be started, thus maximizing observing time.

The CCD read out, transmission down the fiber, DMA into VME-bus memory in the crate, re-transmission down the Ethernet, and display on the instrument computer are all overlapped into one big pipeline. Provided that the aggregate pixel data rate from the Leach controller remains below the effective Ethernet bandwidth (currently about 450 kilopixels/second), the Ethernet does not introduce any significant delay in the receipt of data by the instrument computer. For both Keck first-generation optical instruments (HIRES and LRIS), the aggregate pixel data rate (about 30 to 120 kilopixels/second) will remain well below that bandwidth limitation.

Compared to many of the interfaces to the Leach system described earlier in this section, the interface used by the Keck CCD DAS appears very expensive, bulky, and complex. Its total bandwidth is constrained by the Ethernet, and this could become a problem for future instruments involving large mosaics or more rapid readout-amplifier sampling rates. Nonetheless, the existing Keck interface to the Leach CCD controller offers some important advantages in terms of its potential longevity and its ability to prevent data loss and minimize loss of observing time in the event of instrument computer problems that occur during CCD readout.

3.3. Minimizing loss of data and observing time from instrument computer crashes

It is an unfortunate reality of observing that instrument computers can and do crash. If this occurs during a CCD readout, it often means the loss of part or all of the data from that exposure. From the viewpoint of an observatory, given the nightly cost of operating a telescope like the Keck 10-m, such a loss may translate into a significant sum. From the viewpoint of the observer whose data is lost, such a loss may represent catastrophe.

Instrument computers crash for a variety of reasons, many of which are hardware-related. Since instrument computers are often burdened with lots of power-hungry peripherals, it is sometimes impractical to connect them to battery-backup power, and they are thus susceptible to power glitches and failures. In addition, these peripherals often involve lots of moving parts (e.g., disk drives, tape drives), and are subject to various mechanical failures (e.g., head crashes, tape jams). These failures often require the system to be power-cycled to swap components, or at least rebooted. Also, since users are in constant contact with the instrument computer, it is susceptible to derangement by electrostatic discharge (ESD), which is especially a problem in the dry mountain air where these computers are typically operated.

But instrument computers also crash (or at least require rebooting) for a variety of software reasons. They typically run very complex multi-user operating systems which are never stable nor fully-debugged. New releases of operating system software and major application packages (e.g., IRAF), while solving some old bugs, usually introduce many new ones. In addition, it is difficult to predict or control what other unknown software users will introduce onto the machine, either home-grown or public-domain software obtained off the network, and any of these can introduce subtle bugs. While such bugs may not crash the system outright, they may result in various resource exhaustion problems (e.g., filled disk partitions, consumption of all process slots) which so paralyze the system that it must be rebooted anyway. Usually, such system reboots not only lose any data which may be in the process of being read out, but they also result in significant loss of observing time, since subsequent exposures cannot be initiated until the reboot completes. If the instrument computer is configured with lots of disk drives whose contents must undergo file system consistency checks, this may take tens of minutes.

The Keck interface to the Leach CCD controller chassis avoids these problems by buffering the CCD image in the VME-bus memory of the data capture computer. Since both the Leach controller and the data capture computer will be on battery-backup power, they should be immune to most power glitches and outages. Because both are typically out of reach of the observer, they should also be less susceptible to ESD. Neither has any peripherals with moving parts, so they should be immune to disk head crashes and tape jams. Furthermore, the software in both is significantly less complex than the multi-user systems and massive application packages which run on the instrument computer. That software should also be considerably more stable, and immune to user perturbation, since users do not log in directly to either the Leach CCD controller or the data capture computer.

In the event that an instrument computer either temporarily hangs, crashes, or needs to be forcibly rebooted while the CCD is being readout, no data will be lost, because it is buffered in the data capture computer. Once the instrument computer either recovers or reboots, the data capture computer will resend as much data as needed to insure that the complete image is successfully received. In the case of a hard failure of a given instrument computer, or if the time required to reboot it is excessive, it is a simple matter to have the data capture computer send the image to any backup instrument computer on the network. In fact, the entire Keck CCD DAS can be switched over to a backup machine in less than a minute, without the need for any recabling, rebooting, or power-cycling of equipment. Thus, data loss is avoided, and loss of observing time is minimized.

In the case of instrument computer problems, most of the previously described interfaces to the Leach CCD controller cannot avoid either a partial data loss, or a significant loss of observing time if the instrument computer must be rebooted. The proposed SCSI interface holds some promise in this regard if it can be designed to buffer a complete image, and retain it across a reboot of the instrument computer to which it is attached. However, in the event of a hard failure of the instrument computer, data loss would most likely occur, since the SCSI interface unit would need to be power-cycled before it could be moved to a backup instrument computer. Alternatively, this SCSI interface could be attached directly to the SCSI port on the Sparc-1E in the Keck data capture computer, simply replacing the existing custom interface board and IKON DR11-W DMA controller. In this way, the existing crash recovery capabilities of the Keck CCD DAS could be retained, at the expense of losing the increased bandwidth that would otherwise be achieved were the SCSI interface attached directly to the instrument computer.

4. Next generation CCD DAS at Lick Observatory

While those portions of the Lick CCD DAS which are most visible to the observer (e.g., instrument computers, user interfaces, data displays) will probably change very little in the near term, it is fairly certain that over the next year the Leach CCD controllers will begin to replace the existing Lick CCD controllers, both at the Lick telescopes and in our CCD Detector Laboratory. What is less clear is the particular type of interface that will be used to interface the Leach CCD controllers to our instrument computers.

One option that is currently being evaluated is Leach's recently-released VME-bus DMA controller board. (A SunOS 4.1e device driver for the Leach

DMA board has been provided by Steve Smith at CFHT, where the Leach DMA board is also being used.) We are testing this board in a data capture computer similar to the one employed in the Sparc-based system recently installed at the CAT telescope and which was previously described in section 2.4. In this test system, Leach's VME-bus DMA controller board replaces the VME board used to operate the Lick serial multiplexer link that connects to the existing Lick CCD controllers. Should these tests prove successful in the lab, the CAT telescope will provide the next likely test bed to determine how the overall system performs under actual observing conditions. Another option which will likely be evaluated is the proposed SCSI interface, provided that funding for that development effort is approved.

In making the transition from the Lick CCD controllers to the Leach controllers, an initial concern was whether a convenient, safe, and efficient means could be developed to allow CCD waveforms to be dynamically adjusted in real-time using the Leach controller, since adjustment of these waveforms is a frequent operation in our CCD detector lab. With the existing Lick controllers, the various CCD clocking and bias voltage levels are set by potentiometers, and can quickly be adjusted using a screwdriver while using an oscilloscope to watch the resulting effect on the CCD video signal. However, changes to waveform timing require recompilation, burning new UV-erasable EPROM chips, and installing these chips into the controller, which typically requires at least 10-15 minutes. Since the waveforms generated by the Leach controllers are set by programmable DACs, and since new waveform tables can be quickly downloaded via the fiber optic link, the potential exists for fully software controlled, dynamically adjustable waveforms.

To realize this potential, Stover has implemented a CCD waveform generation tool, wavegen (Stover 1991). Wavegen provides an X11/Motif-based graphical user interface which allows the user to draw new CCD waveforms, and to easily manipulate both the timing and voltage levels of existing waveforms. Wavegen also enforces CCD-specific voltage limits, to prevent the user from accidentally generating levels which might damage the chip, and also enforces timing constraints imposed by the Leach controller hardware. Once the user is satisfied with a given set of waveforms, wavegen produces an ASCII source file in DSP56001 assembler format which can be assembled to generate the appropriate waveform tables. While this makes the generation of these tables simpler, safer, and better documented, it still does not result in real-time waveform adjustment. However, it has reduced the time required to change a waveform (in either timing, voltage, or both) to under one minute, and that reduction has already markedly increased our efficiency in using the Leach CCD controllers to characterize the performance of new detectors.

Wavegen also provides a mechanism by which it can broadcast (via the MUSIC system) change notification event messages whenever the user makes any adjustment to a waveform. These messages can be monitored by another process, wavemon, which collects the changes and downloads an updated set of waveforms to the Leach CCD controller whenever the user requests. A preliminary version of wavemon is now being tested, and should be fully operational early next year. Once that is finished, it will be possible to safely and efficiently adjust Leach CCD controller waveforms in real-time.

5. Conclusions

Although predicting future trends is always somewhat problematical, if we use our experience at Lick over the past 12 years as a guide, it is likely that instrument computer hardware and software will continue to change much more rapidly than CCD controller hardware and software. That trend should be seriously considered when selecting an overall architecture for a CCD DAS.

The need for frequent re-implementation of the interface between the instrument computer and the CCD controller can be reduced by isolating the custom parts of that interface into a separate data capture computer, and by insuring that the data capture computer connects to a basically 'off-the-shelf' instrument computer using a widely-accepted (and hopefully long-lived) industry standard interface such as Ethernet or SCSI. In some implementations, such as the Keck CCD DAS, this data capture computer should significantly reduce both the loss of data and observing time that currently results from instrument computer failures.

The Leach CCD controller is gaining considerable acceptance in Astronomy, and may become something of a standard. All users of this controller will benefit from continued discussions regarding the best means of interfacing to this system, and from sharing experience gained in the operational details of these controllers.. Efforts are now in progress to organize an informal users group, and to continue such discussions via electronic mail.

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