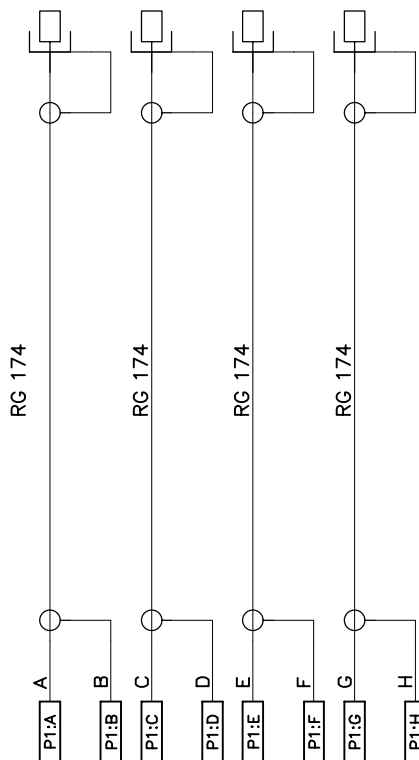


BNC Connectors at Interconnect Box



60 Pin Header on interconnect card

1	SGND	J1:1
2	SGND	J1:2
3	SGND	J1:3
4	SGND	J1:4
5	SGND	J1:5
6	S3(A)	J1:6
7	S2(LA)	J1:7
8	P3	J1:8
9	P2(A)	J1:9
10	S1(RA)	J1:10
11	S1(LB)	J1:11
12	S1(RB)	J1:12
13	HEATER	J1:13
14	S1(LA)	J1:14
15	HEATER_RETURN	J1:15
16	TEMP_ANODE	J1:16
17	TEMP_CATHODE	J1:17
18	S2(RB)	J1:18
19	S2(RA)	J1:19
20	S2(LB)	J1:20
21	VSUB	J1:21
22		J1:22
23		J1:23
24	SGND	J1:24
25	SGND	J1:25
26	P2(B)	J1:26
27	SGND	J1:27
28	P1(B)	J1:28
29	SGND	J1:29
30	SGND	J1:30
31	SGND	J1:31
32	SGND	J1:32
33	P1(A)	J1:33
34	S3(B)	J1:34
35	TC(A)	J1:35
36	TC(B)	J1:36
37	SW(LA)	J1:37
38	SW(RA)	J1:38
39	SW(LB)	J1:39
40	SW(RB)	J1:40
41	RD(LA)	J1:41
42	RD(RA)	J1:42
43	RD(LB)	J1:43
44	RD(RB)	J1:44
45	DC(A)	J1:45
46	DC(B)	J1:46
47	OG(LA)	J1:47
48	OG(RA)	J1:48
49	OG(LB)	J1:49
50	OG(RB)	J1:50
51	OD(LA)	J1:51
52	OD(RA)	J1:52
53	OD(LB)	J1:53
54	OD(RB)	J1:54
55	RG(LA)	J1:55
56	RG(RA)	J1:56
57	RG(LB)	J1:57
58	RG(RB)	J1:58
59	DC(A)	J1:59
60	DC(B)	J1:60

Bendix PT06A-24-61S to DEWAR

*1: These wired shown connected to B,D,F and H, but in reality covered with heat shrink and left unconnected.

REVISION		UNIVERSITY OF CALIFORNIA LICK OBSERVATORY		MOS Dewars 60 pin to 61 pin Cable	
2/18/99 CONVERTED TO ACCEL EDA (V14)		DES'N BY: L. Bresee	ORIGIN DATE: 11-05-97	DWG. NO.	NUM. 1 OF 1
		DRAWN BY:	MODIFY DATE: 2/18/99	EL-1245-1W	
		PATH: MOS/IntCable	REV. A		