e2v technologies

CCD203-82
Back Illuminated
4096 x 4096 Pixel Scientific CCD Sensor

FEATURES

- 4096 x 4096 Pixels
- 12.0 µm Square Pixels
- 49.2 mm x 49.2 mm Image Area
- Back Illuminated for High Spectral Response
- 4-Phase Image Section Clocking
- Very Low Noise Output Amplifiers
- Flatness better than ±15 µm
- Compact Buttable Package
- 100% Active Area
- All specifications apply at –100 °C
- Non inverted mode operation

APPLICATIONS

- Astronomy
- Scientific Imaging and Spectroscopy

INTRODUCTION

This newly developed device is based on the well-established CCD42 and CCD44 family of scientific CCD Sensors. The CCD203 has been designed to provide a large image area for demanding astronomical and other scientific imaging applications. The back-illuminated spectral response combined with very low read-out noise give exceptional sensitivity. The device has been designed for applications such as low-noise spectroscopy and broadband photometric imaging.

DESCRIPTION

The sensor is arranged as a nominally 4096 x 4096 array, with split frame architecture, two output registers, and four outputs. The sensor may be read out from one, two or four outputs. Square 12 µm pixels allow high-resolution imaging.

There are extra rows of pixels such that the total number is actually 4096 horizontal by 2 x 2068 = 4136 vertical.

The register and output capacities are designed to allow full capacity 2 x 2 binning, so that the device may be operated efficiently as a 2048 x 2068 24 µm-pixel imager if desired.

The output amplifier is designed to give minimum read-out noise at low pixel rates as well as low noise at pixel rates as high as 3 MHz. The low output impedance of approx. 350 Ω simplifies the interface with external electronics. Dummy outputs are also available to facilitate common mode rejection.

The read-out register has a gate controlled dump drain to allow fast dumping of unwanted data. The register is designed to accommodate 2 image pixels of charge and a summing well is provided capable of holding 4 image pixels. The output amplifier has a switchable gate (OG2) to enable the responsivity to be reduced to allow the reading of such large (binned) charge packets.

The package provides guaranteed flatness at cryogenic temperatures, as well as a compact footprint. Connections are made at the top and bottom of the device, so that the sides may be close butted if needed. Buttable packages require careful handling. The devices are shipped in a protective box, but do not have a cover window. Consult e2v technologies for advice.

Alternative AR-coatings, deep depletion silicon, and inverted-mode options may be available; consult e2v technologies.

Specifications are guaranteed and tested at –100 °C.

GENERAL DATA

Format

Image area	49.2 mm x 49.2 mm
Active pixels:	
horizontal	4096
vertical	2068+2068
Pixel size	12 µm x 12 µm
Number of output amplifiers	4
Number of serial registers	2
Number of serial under-scan pixels	50
Fill factor (%)	100

Package

Format	metal pack with two flex-cable connectors
Size	51.5 mm x 61.5 mm
Weight	260 g (approx)
Focal plane height, above base	14 ± 0.02 mm
Surface flatness	30 µm peak-to-valley
Connectors	two 37-way micro-D
Inactive edge spacing (nominal; 50 µm tolerance):	
each side (with covers)	1300 µm
each side (without covers)	800 µm
each connector edge	6.2 mm

An integral temperature sensor can be fitted. If required, consult e2v technologies.

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PERFORMANCE (at 173 K unless stated)

Parameter	Min	Typical	Max	Units	Notes
Peak charge storage (image)	130,000	175,000	-	e^-/pixel	Note 1
Peak charge storage (register)	-	750,000	-	e^-/pixel	
Output node capacity:					Note 2
OG2 low (mode 1)	-	400,000	-	e^-	
OG2 high (mode 2)	-	1,200,000	-	e^-	
Output amplifier responsivity:					Note 2
mode 1	3	4.5	-	µV/e^-	
mode 2	-	1.5	-	µV/e^-	
Peak output voltage	-	1.8	-	V	
Readout noise	-	3	4.5	e^- rms	Note 3
Readout frequency	20	50	3000	kHz	Note 4
Dark signal:					Note 5
at 173 K	-	3	-	e^-/pix/hr	
at 153 K	-	0.01	2	e^-/pix/hr	
Charge transfer efficiency :					Note 6
parallel	99.9990	99.9995	100	%	
serial	99.9990	99.9995	100	%	
Spectral range	300	-	1060	nm	
Peak quantum efficiency	-	90	-	%	

Notes

General: **Grade-5** devices are fully functional devices for set-up purposes only. Image quality is below that of science-grades, and all other performance parameters may not be tested.

1. Signal level at which resolution begins to degrade; image area charge will spill into the following row.
2. Operation of the OG2 gate modifies the output node. OG2= "low" (mode 1) gives high responsivity and lowest noise. OG2 = "high" (mode 2) gives more charge-handling capacity (e.g. for pixel binning). See also note 9.
3. Measured with correlated double sampling using a 10 µs integration period (mode 1). The serial register is reverse-clocked.
4. See page 4 for a typical noise versus frequency graph. Lowest noise is achieved at read-out rates up to about 20 kHz. The register will transfer charge at much higher frequencies, but the output amplifier slew rate (with 10 pF external load) will limit the maximum frequency of operation to about 2.5 – 3.0 MHz.
5. The dark signal is a strong function of temperature. The typical average (background) dark signal at any temperature T (Kelvin) between 150 K and 300 K may be determined using: $Q_d/Q_{do} = 122T^3e^{-6400/T}$, where Q_{do} is the dark signal at 293 K. Note that this is typical performance and some variation may be seen between devices. Reducing the operating temperature may be desirable in some cases. Some reduction in dark current may be obtained with a high substrate voltage (9V).
6. Measured with an Fe55 X-ray source. CTE is quoted for the complete clock cycle (all phases, not per phase).

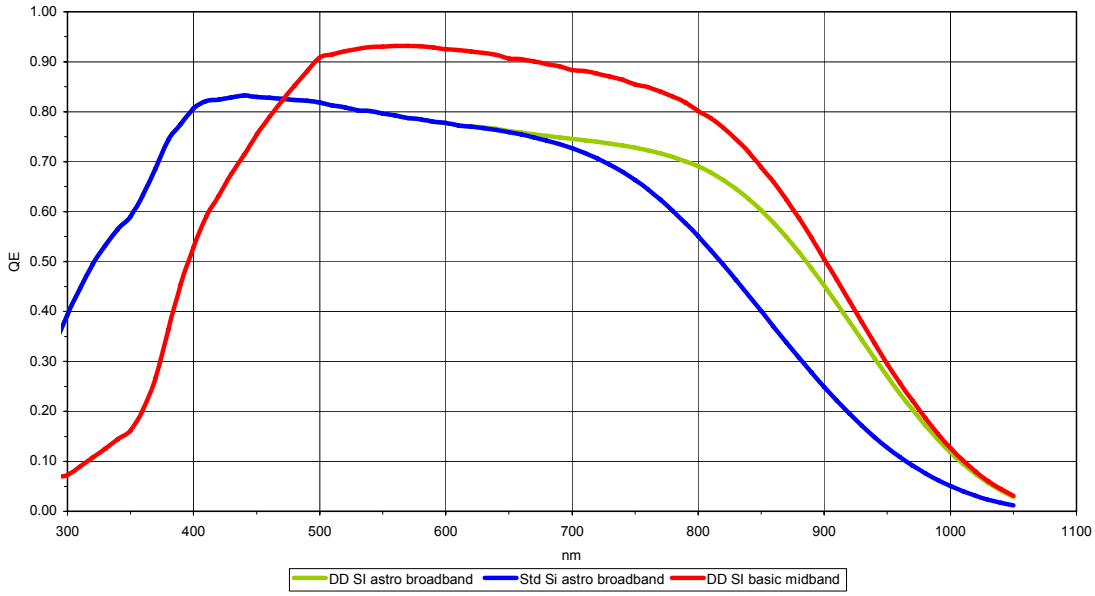
SPECTRAL RESPONSE AT 173 K

The table below indicates guaranteed (minimum) values for blue and red variants.

Wavelength (nm)	Spectral Response		Max Pixel Response Non-Uniformity PRNU (1σ)	Units
	Minimum QE	Minimum QE		
	Standard Silicon, Astro-Broadband (Blue)	Deep depletion, Basic Mid-band (Red)		
350	40	-	-	%
400	70	20	3	%
500	80	75	-	%
650	75	80	3	%
900	25	50	5	%

See graph on page 3 for typical spectral response.
Devices with alternative spectral response may be available; consult e2v technologies for details.

TYPICAL QUANTUM EFFICIENCY AT -100 °C



The graph indicates typical spectral response. Other variants can be supplied (consult e2v technologies).

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

Grade	0	1	2	3	0	1	2	3
	Guaranteed Specifications				Typical Values			
Column defects - black or white	3	8	16	30	0	~2	<6	<10
White spots	300	600	1200	2000	<100	<200	<400	<600
Total (black and white) spots	900	1500	2000	3000	<100	<300	<600	<1000
Traps	20	20	40	60	<5	<10	<10	<20

Grades 1 and 2 are the default for science use.
Grades 0 and 3 may have limited availability.
Grade 5 devices are fully functional, but with an image quality below that of grade 3, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots Are counted when they have a generation rate equivalent to 300 e^-/pixel/minute at 173 K. (This is equivalent to 100 e^-/hr at 153K). Temperature dependence is the same as for dark current; see note 5 above.

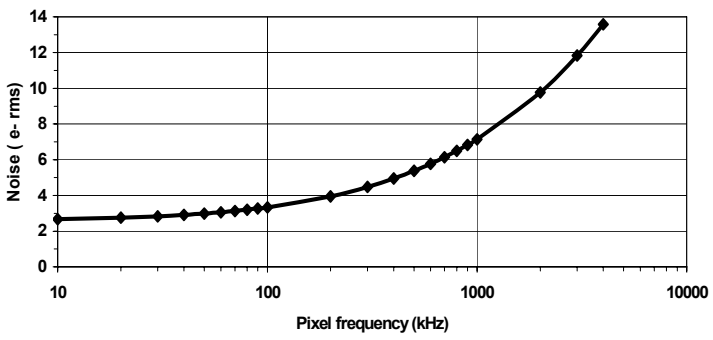
Black spots Are counted if the response is less than 50% of the local mean signal.

Column defects A column that contains at least 100 white or dark pixel defects.

Traps Pixels where charge is temporarily held, if they have a capacity greater than 200 e^-.

TYPICAL OUTPUT AMPLIFIER NOISE

(Measured using clamp and sample, temperature range 150 – 230 K)



ARCHITECTURE

See later pages for read-out modes and clocking schemes.

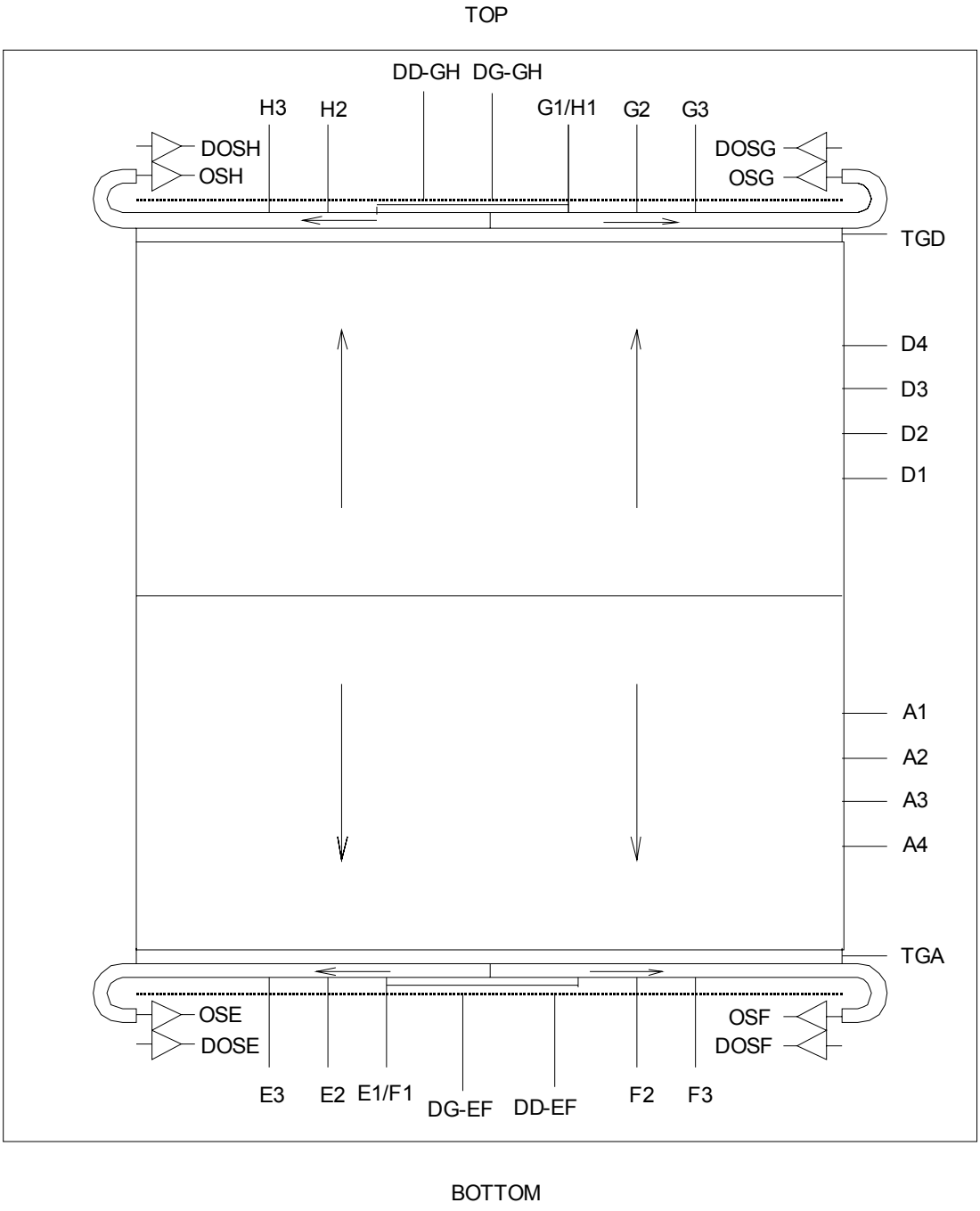
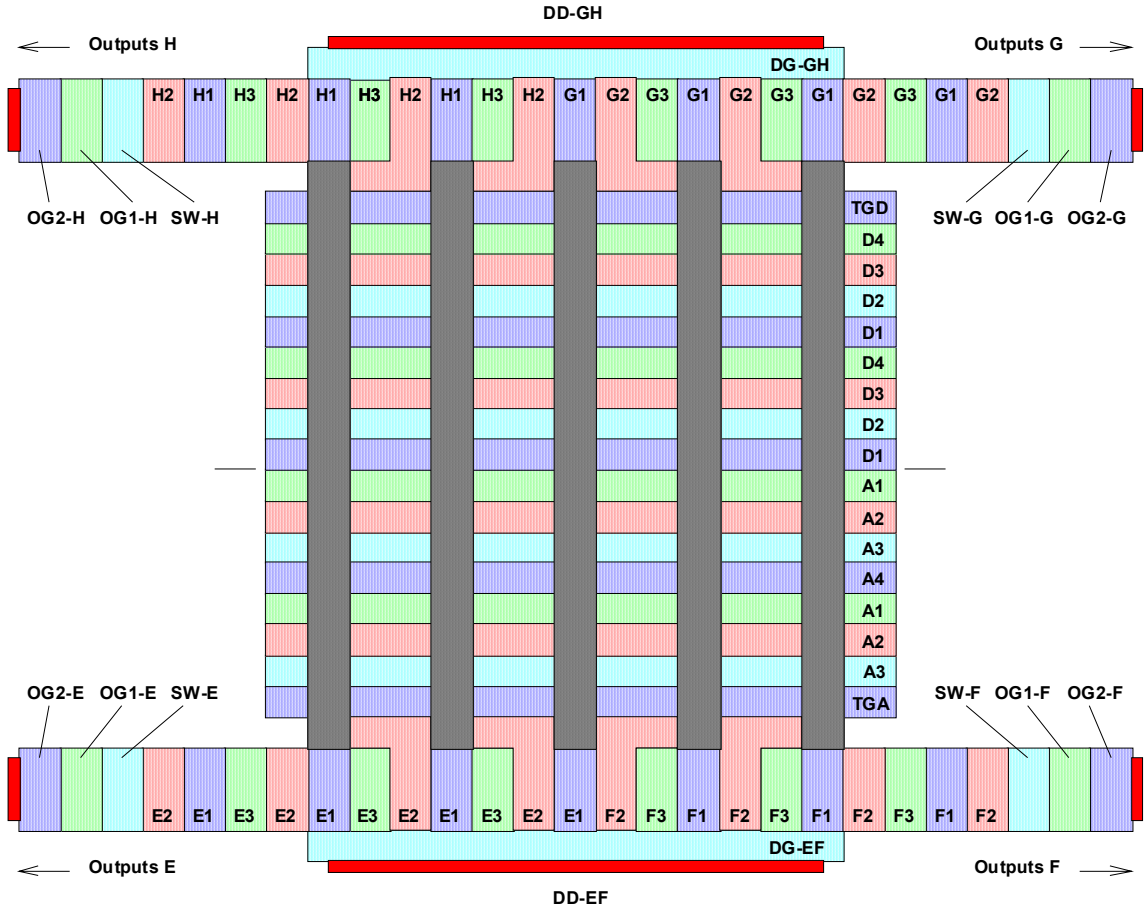


Image sections A & D each have a total of 4096 (H) X 2068 (V) pixels. Serial registers have 50 pre-scan elements.

For full frame read-out from one corner the number of clock cycles must exceed 4146 X 4136.

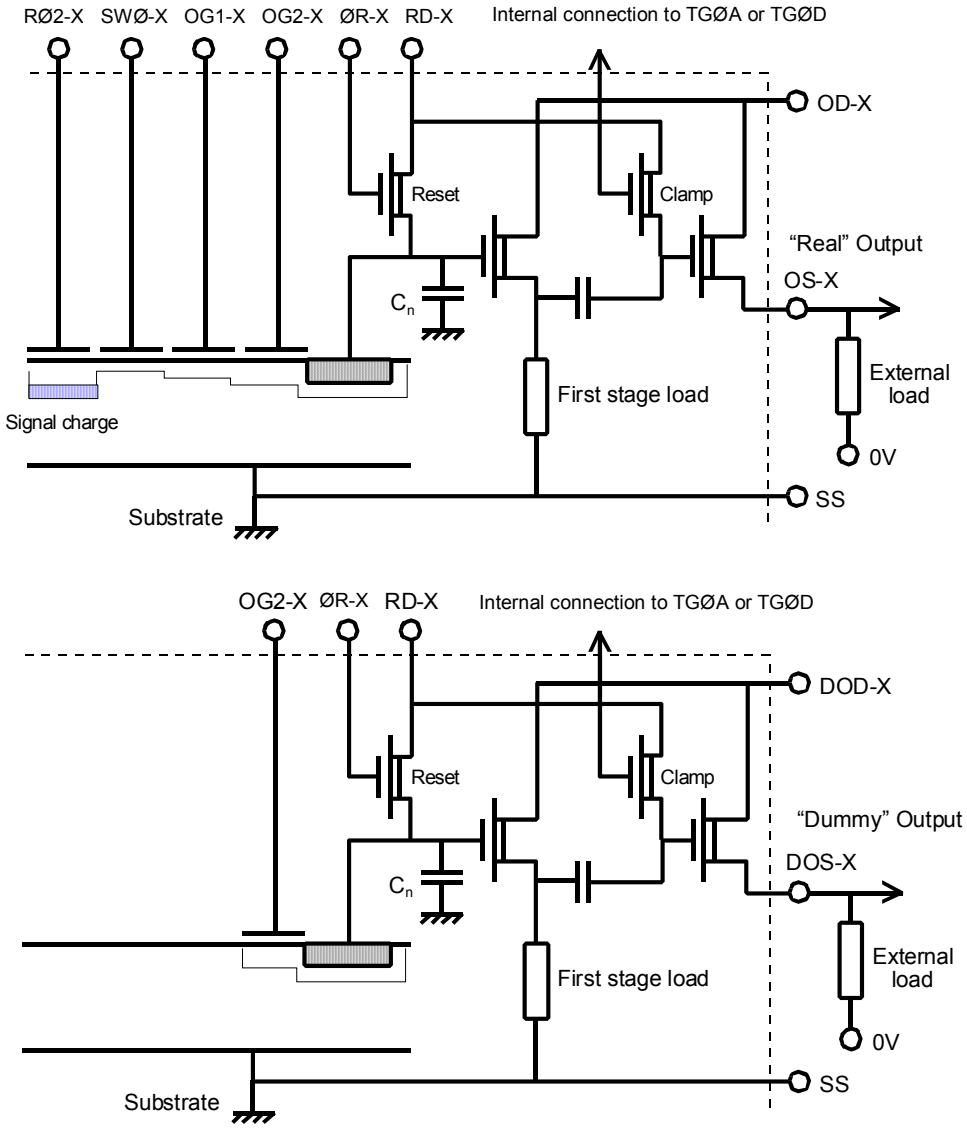
ARRANGEMENT OF ELECTRODES

As viewed from the back-face through the thinned silicon



OUTPUT CIRCUITS (active “REAL” and “dummy” outputs)

X designates a specific output, namely E, F, G or H



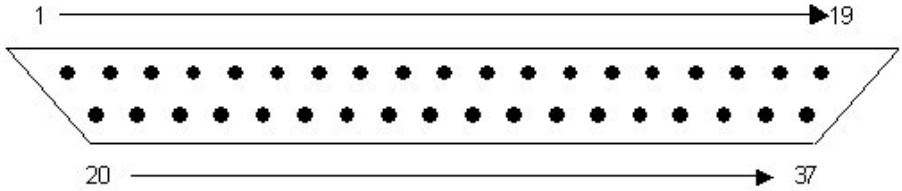
The first stage load of each output (real or dummy) draws a quiescent current of approximately 0.2mA via SS.

The output circuit consists of two capacitor-coupled source-follower stages. The particular design has a very high responsivity to give lowest noise. The load for the first stage is on-chip and that for the second stage is external, as next described. The dc restoration circuitry requires a pulse at the start of line read-out, and this is automatically obtained by an internal connection to the adjacent transfer gate, TG. Transferring a line of charges to the register thus automatically activates the circuitry, n.b. TG pulses still need to be applied at similar intervals if only the register and/or output circuit are being operated, e.g. for test or characterisation purposes.

If any output is to be powered down, it is recommended that OD or DOD is either set to SS voltage, taking care that the maximum ratings are never exceeded, or simply disconnected. If external loads return to a voltage below SS they should also be disconnected.

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

There are two flexible connectors terminating in 37-pin micro D's. Connector 1 is attached to image section A and register EF, and connector 2 is attached to image section D and register GH (see Device Architecture and Package Detail diagrams). The pin-outs of the connectors (viewed facing the pins) are the same EXCEPT for the order of the image clocks. The CCD is not electrically connected to the metal package.



The tables below give the pin-outs for each connector. Note that the hyphenated suffix symbols (e.g. ØR-**E**) indicate to which amplifier the CCD pin relates. Those ending with an **A** or a **D** refer to a specific half of the image.

The connector is a 37 pin micro D type, Glenair part number DCDM 37P.

Clock pulse low levels = 0 V (± 0.5 V), except RØ and SW low = +1 V (± 0.5 V).

CONNECTOR 1

MICRO D PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 7)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	N.C.	Not Connected	N/A	N/A	N/A	N/A
2	DOD-E	Dummy Output Drain (E)	26	see note 8	29	-0.3 to +35
3	ØR-E	Reset Gate (E)	8	10	13	±20
4	OD-E	Output Drain (E)	26	see note 8	29	-0.3 to +35
5	SS	Substrate (see note 12)	0	0	10	N/A
6	OG1-E	Output Gate 1 (E)	1	4	4	±20
7	E2	Register Clock Phase 2 (E)	8	10	13	±20
8	EF1	Register Clock Phase 1 (Register EF)	8	10	13	±20
9	A3	Image Area Clock Phase 3 (A)	8	10	13	±20
10	N.C.	Not Connected	N/A	N/A	N/A	N/A
11	A2	Image Area Clock Phase 2 (A)	8	10	13	±20
12	TGA	Transfer Gate (A)	8	10	13	±20
13	F3	Register Clock Phase 3 (Register F)	8	10	13	±20
14	SWF	Summing Well Gate (F)	8	10	13	±20
15	OG2-F	Output Gate 2 (F) (see note 9)	1	5	5	±20
16	OS-F	Output Source (F)		(see note 11)		N/A
17	RD-F	Reset Drain (F)	15	see note 8	19	-0.3 to +25
18	SS	Substrate (see note 12)	0	0	10	N/A
19	DOS-F	Dummy Output Source (F)		(see note 11)		N/A
20	DOS-E	Dummy Output Source (E)		(see note 11)		N/A
21	SS	Substrate (see note 12)	0	0	10	N/A
22	RD-E	Reset Drain (E)	15	see note 8	19	-0.3 to +25
23	OS-E	Output Source (E)		(see note 11)		N/A
24	OG2-E	Output Gate 2 (E) (see note 9)	1	5	5	±20
25	SWE	Summing Well Gate (E)	8	10	13	±20
26	E3	Register Clock Phase 3 (Register E)	8	10	13	±20
27	DG-EF	Dump Gate (EF) (see note 10)	0	0	15	±20
28	N.C.	Not Connected	N/A	N/A	N/A	N/A
29	A1	Image Area Clock Phase 1 (A)	8	10	13	±20
30	A4	Image Area Clock Phase 4 (A)	8	10	13	±20
31	DD-EF	Dump Drain (EF)	20	24	29	-0.3 to +25
32	F2	Register Clock Phase 2 (F)	8	10	13	±20
33	OG1-F	Output Gate 1 (F)	1	4	4	±20
34	SS	Substrate (see note 12)	0	0	10	N/A
35	OD-F	Output Drain (F)	26	see note 8	29	-0.3 to +35
36	ØR-F	Reset Gate (F)	8	10	13	±20
37	DOD-F	Dummy Output Drain (F)	26	see note 8	29	-0.3 to +35

CONNECTOR 2

MICRO D PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 7)			MAXIMUM RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
1	N.C.	Not Connected	N/A	N/A	N/A	N/A
2	DOD-G	Dummy Output Drain (G)	26	see note 8	29	-0.3 to +35
3	ØR-G	Reset Gate (G)	8	10	13	±20
4	OD-G	Output Drain (G)	26	see note 8	29	-0.3 to +35
5	SS	Substrate (see note 12)	0	0	10	N/A
6	OG1-G	Output Gate 1 (G)	1	4	4	±20
7	G2	Register Clock Phase 2 (G)	8	10	13	±20
8	GH1	Register Clock Phase 1 (Register GH)	8	10	13	±20
9	D2	Image Area Clock Phase 2 (D)	8	10	13	±20
10	N.C.	Not Connected	N/A	N/A	N/A	N/A
11	D3	Image Area Clock Phase 3 (D)	8	10	13	±20
12	TGD	Transfer Gate (D)	8	10	13	±20
13	H3	Register Clock Phase 3 (Register H)	8	10	13	±20
14	SWH	Summing Well Gate (H)	8	10	13	±20
15	OG2-H	Output Gate 2 (H) (see note 9)	1	5	5	±20
16	OS-H	Output Source (H)		(see note 11)		N/A
17	RD-H	Reset Drain (H)	15	see note 8	19	-0.3 to +25
18	SS	Substrate (see note 12)	0	0	10	N/A
19	DOS-H	Dummy Output Source (H)		(see note 11)		N/A
20	DOS-G	Dummy Output Source (G)		(see note 11)		N/A
21	SS	Substrate (see note 12)	0	0	10	N/A
22	RD-G	Reset Drain (G)	15	see note 8	19	-0.3 to +25
23	OS-G	Output Source (G)		(see note 11)		N/A
24	OG2-G	Output Gate 2 (G) (see note 9)	1	5	5	±20
25	SWG	Summing Well Gate (G)	8	10	13	±20
26	G3	Register Clock Phase 3 (Register G)	8	10	13	±20
27	DG-GH	Dump Gate (GH) (see note 10)	0	0	15	±20
28	N.C.	Not Connected	N/A	N/A	N/A	N/A
29	D4	Image Area Clock Phase 4 (D)	8	10	13	±20
30	D1	Image Area Clock Phase 1 (D)	8	10	13	±20
31	DD-GH	Dump Drain (GH)	20	24	29	-0.3 to +25
32	H2	Register Clock Phase 2 (H)	8	10	13	±20
33	OG-1H	Output Gate 1 (H)	1	4	4	±20
34	SS	Substrate (see note 12)	0	0	10	N/A
35	OD-H	Output Drain (H)	26	see note 8	29	-0.3 to +35
36	ØR-H	Reset Gate (H)	8	10	13	±20
37	DOD-H	Dummy Output Drain (H)	26	see note 8	29	-0.3 to +35

NOTES

7. For the clock connections the table indicates only the high levels for the clock pulses.

To ensure that any device can be operated the camera should be designed so that any value in the range “min” to “max” can be provided. All operating voltages are with respect to image clock low (nominally 0V).

The clock pulse low levels should be in the range 0 ± 0.5V for image clocks. The register and SW clock low level should be +1V higher. Reset clock low may be nominally 0V or +1V.

This data sheet adopts parallel clock low voltage level as 0V, with all other signals relative to that. The absolute level of all clock & bias rails may be adjusted to suit the needs of the camera system designer, provided that relative levels are maintained. For example, it is acceptable to set the parallel clock low level at –9V with all others levels to match. In this case if Vss=0V this would correspond to operating with a ‘high’ substrate voltage. The specified difference between Vss and all other bias and clock voltages must be maintained. The current load on all output sources should still be set as shown in note 8

8. For Standard silicon (blue) devices: Typical OD= 28V, Typical RD= 18V

   For deep depletion (red) devices: Typical OD= 26.5V, Typical RD= 16.5V

9. OG2 = OG1 + 1 V. For operation in the high responsivity, low noise mode, OG2 should be set to 4 V typical. For operation in the low responsivity, increased charge-handling mode, OG2 should be set to +20 V.

10. Non-charge dumping level shown. For charge dumping, DG should be pulsed to 12 ± 2 V.

11. Do not connect to voltage supply but use a ~5mA current source or a ~5kΩ external load. The quiescent voltage on OS is then about 4 volts above the reset drain voltage for these devices. The current through these pins must not exceed 20mA. Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

12. Vss = 0V is the recommended default value for best charge collection (PSF), especially for the deep depletion chip types. Vss = 9V may give some reduction in dark current, but this is not often required for cryogenic operation.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. Specifically the voltage for all drains (pins 2, 4, 17, 22, 31, 35 and 37) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see note 11) do not flow in the OS or DOS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased d.c.-coupled preamplifier.

Similarly for powering down, the substrate must be taken to zero voltage before the drains.

ELECTRICAL INTERFACE CHARACTERISTICS

Typical Electrode Capacitances (Defined at mid-clock level)

IØ/IØ inter-phase [A and D]	16	nF
IØ/SS [1-A, 3-A, 2-D, 4-D]	36	nF
IØ/SS [2-A, 4-A, 1-D, 3-D]	18	nF
RØ/(SS + DG + OD) [E, F, G, H]	380	pF
Amplifier Output impedance	350	Ω

POWER CONSUMPTION

The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives representative values for the components of the on-chip power dissipation for the case of continuous split-frame line-by-line read-out using both registers and all the output circuits with both real and dummy amplifiers activated. The frequency is that for clocking the serial register and an appropriate value of the amplifier load is utilised in each case.

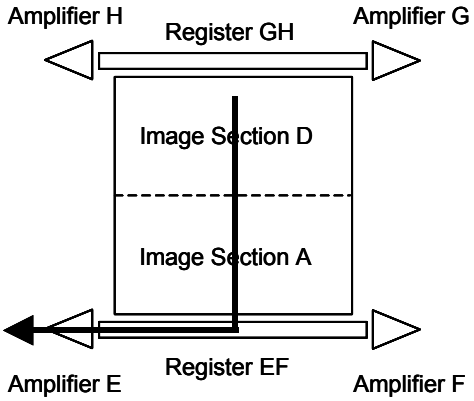
Read-out frequency	**Line time**	**Amplifier load**	**Power dissipation**			
			Amplifiers	**Serial Clocks**	**Parallel clocks**	**Total**
100 kHz	21 ms	10 kΩ	165 mW	17 mW	3 mW	185 mW
1 MHz	2.2 ms	5 kΩ	275 mW	170 mW	30 mW	475 mW
3 MHz	800 µs	2.2 kΩ	525 mW	510 mW	90 mW	1,125 mW

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

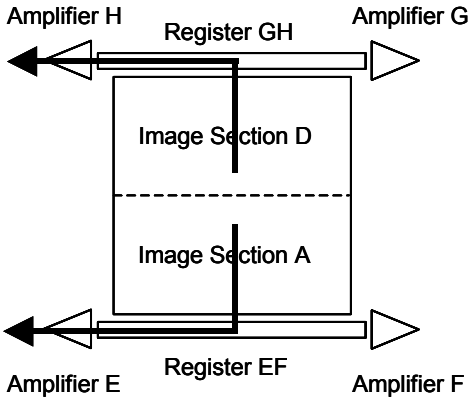
DEVICE OPERATION

FRAME READOUT MODES

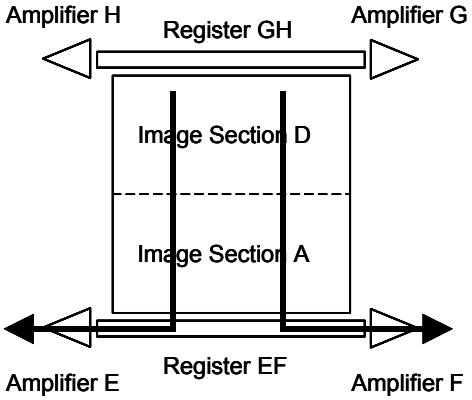
The device can be read out from one, two or four amplifiers. This is determined by the clock pulses applied to the image and register clocks. The diagrams below show what types of transfers are possible.



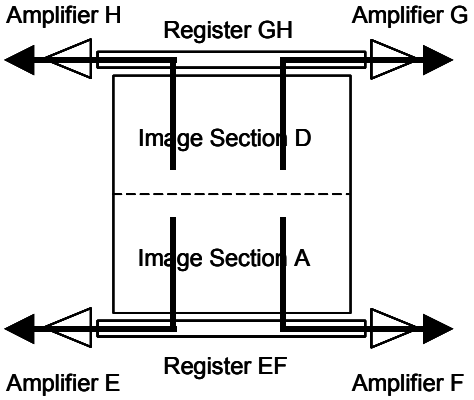
Full frame readout through one amplifier



Split full frame readout through two registers



Full frame readout through two amplifiers on one register



Split full frame readout through four amplifiers

It is recommended that serial phases 2 and 3 are kept high during transfer from the image area to the register. If the applied drive pulses are designated IØ1, IØ2, IØ3 and IØ4, then connections should be made as tabulated below to effect the following directions of transfer.

Read-out mode	Clock Generator Drive Pulse Name:	IØ1	IØ2	IØ3	IØ4	
Split	A section transfer towards E-F register	A1	A2	A3	A4	TGA= IØ4
	D section transfer towards G-H register	D1	D2	D3	D4	TGD= IØ1
Full frame from G-H register	A section transfer towards G-H register	A4	A3	A2	A1	TGA= “low” TGD= IØ1
Full frame from E-F register	D section transfer towards E-F register	D4	D3	D2	D1	TGD= “low” TGA= IØ4

The first two transfer sequences are for split frame readout. The second two are for reversing the transfer direction in either section for full-frame readout to only one of the registers.

Transfer from the image section to the register is via only the RØ2-E, RØ2-F, RØ2-G and RØ2-H electrodes, and these electrodes must be held at clock “high” level during the process. However, also holding the RØ3-E, RØ3-F, RØ3-G and RØ3-H electrodes “high” during this period allows simple transposition of these phases to change the direction of charge transfer in any half-section. Thus if the applied drive pulses are designated RØ1, RØ2 and RØ3, then connections should be made as tabulated below to effect the following directions of transfer.

Clock Generator Drive Pulse Name:	RØ1	RØ2	RØ3
E section transfer towards E output	EF1	E2	E3
F section transfer towards F output	EF1	F2	F3
G section transfer towards G output	GH1	G2	G3
H section transfer towards H output	GH1	H2	H3
E section transfer towards F output	EF1	E3	E2
F section transfer towards E output	EF1	F3	F2
G section transfer towards H output	GH1	G3	G2
H section transfer towards G output	GH1	H3	H2

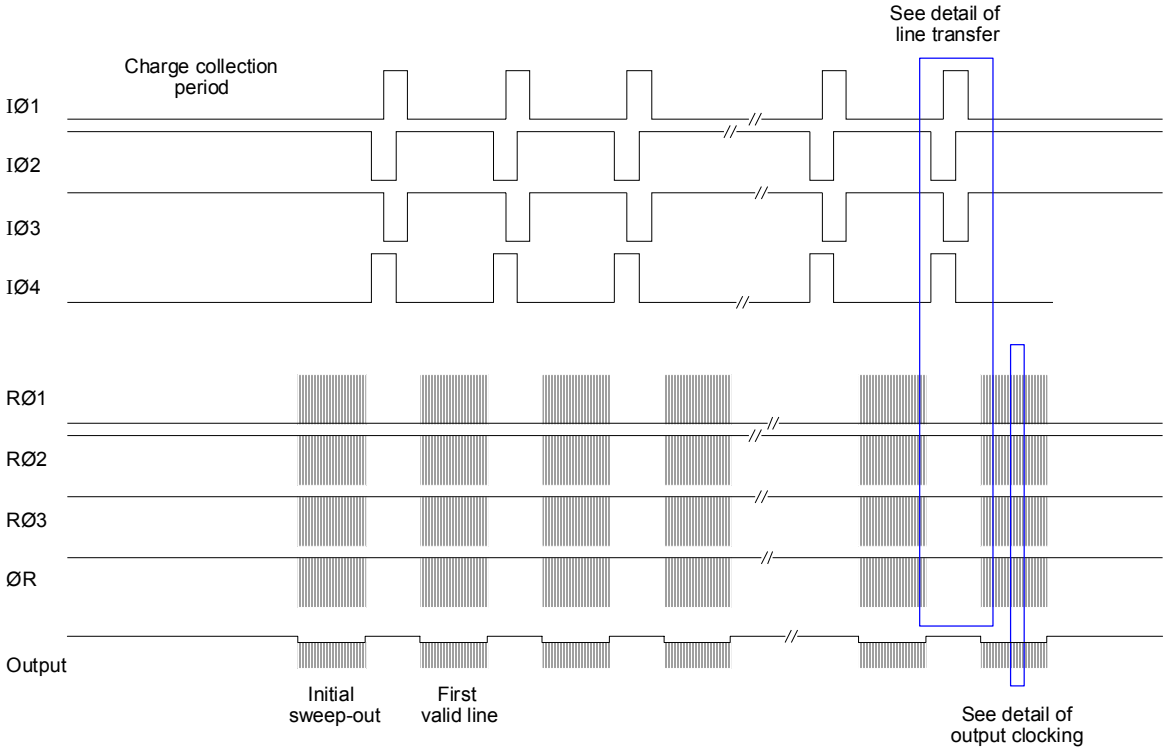
The first four sequences are for split register read-out to all four outputs. The second four are for the reversal of direction in any half section.

The last electrode before the first output gate is separately connected to give the function of a summing well. In normal readout (i.e. if not used for summing) SWE is clocked as E3, SWF as F3, SWG as G3 and SWH as H3. For summing, the selected SW gate is held at clock “high” level for the required number of readout cycles, and then clocked as RØ3 to output charge.

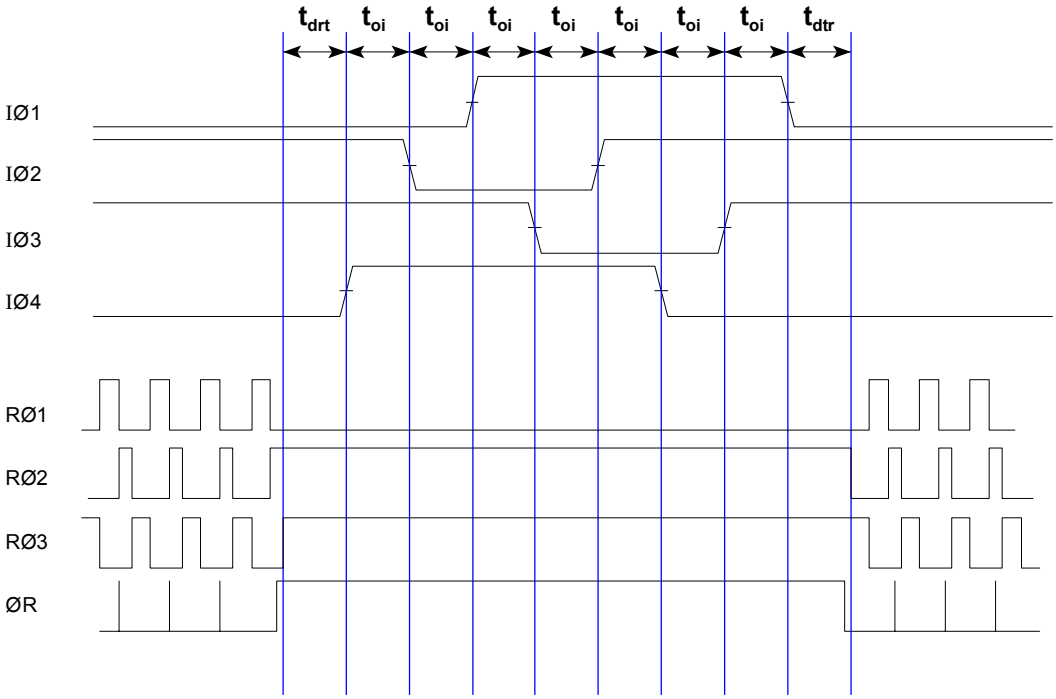
In the diagrams below the transfer gate clocking is not shown. See the read-out mode table above to clock TG with appropriate image clock phase.

TIMING DIAGRAMS

FRAME READOUT TIMING DIAGRAM

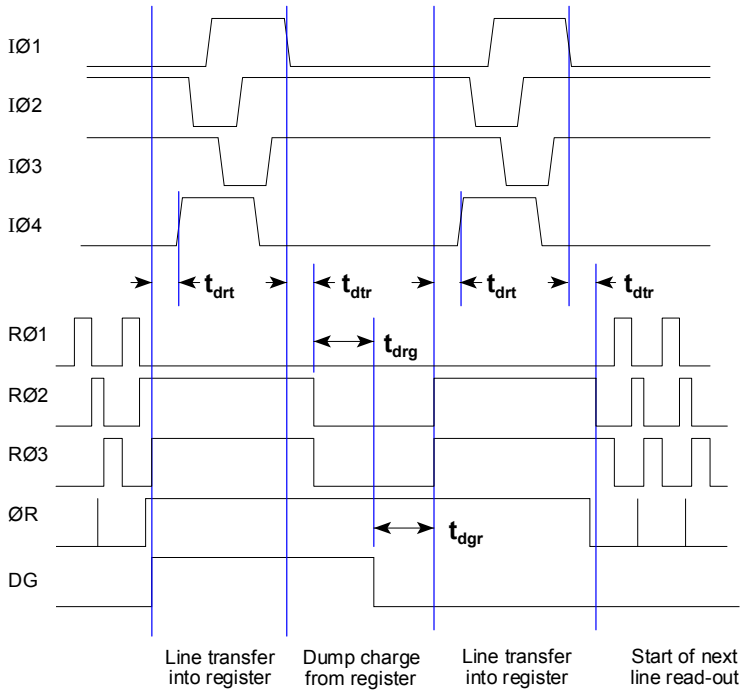


DETAIL OF VERTICAL LINE TRANSFER



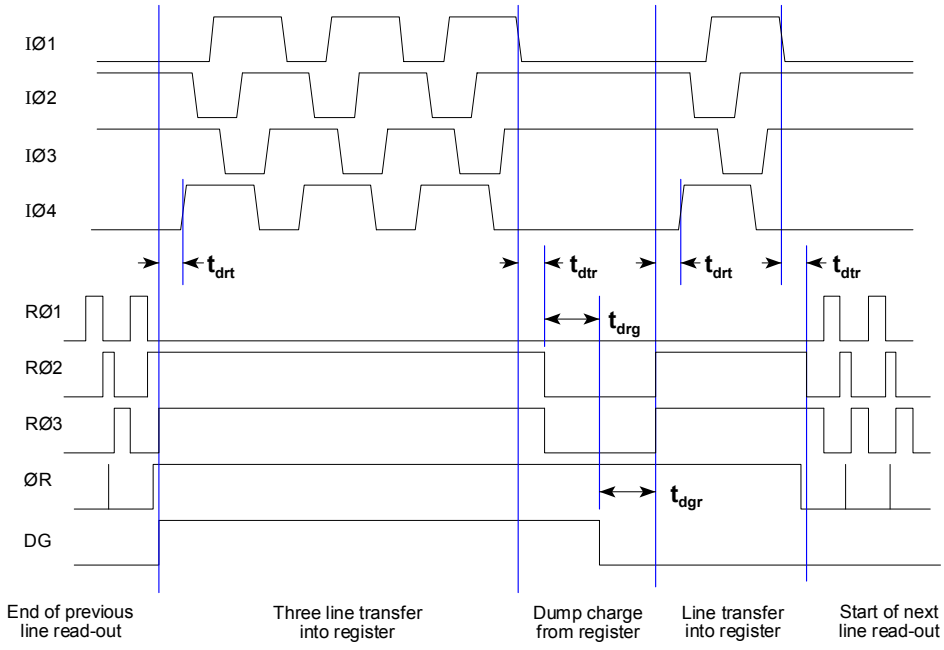
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)

CCD203: 4Ø NIMO Single Line Dump

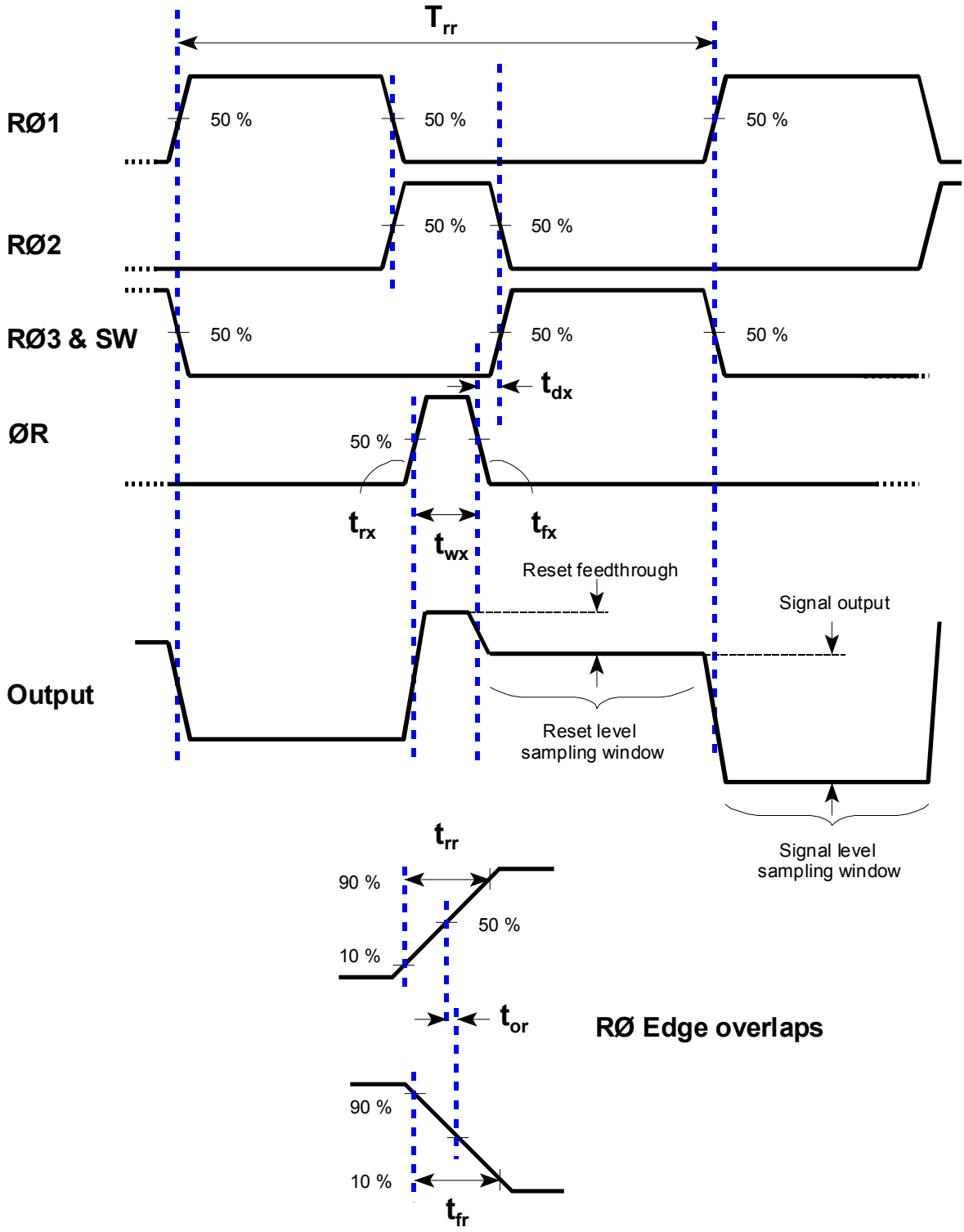


DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump, three shown)

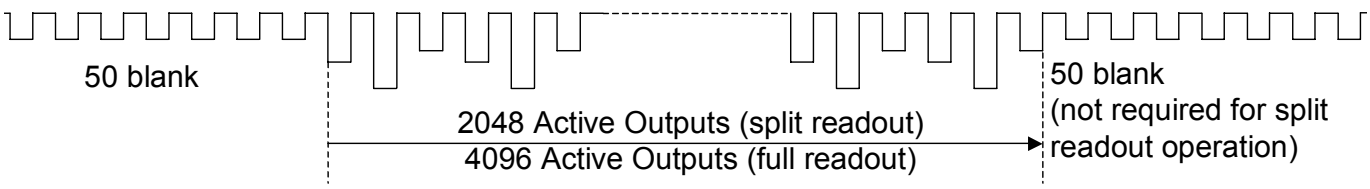
CCD203: 4Ø NIMO Three Line Dump



DETAIL OF OUTPUT CLOCKING



LINE OUTPUT FORMAT



CLOCK TIMING REQUIREMENTS

Symbol	Description	Min.	Typical	Max.	Unit
T_i	Line transfer time (see note 13)	90	90	100 (see note 14)	µs
t_{oi}	Image clock pulse edge overlap	TBD	10	11 (see note 14)	µs
t_{ri}	Image clock and transfer gate pulse rise time	0.2	0.5	0.5 t_{oi}	µs
t_{fi}	Image clock pulse fall time	0.2	0.5	0.5 t_{oi}	µs
t_{tgf}	Transfer gate pulse fall time	5	6	t_{dtr} –2	µs
t_{drt}	Delay time, RØ stop to IØ rising	2	10	11 (see note 14)	µs
t_{dtr}	Delay time, IØ falling to RØ start	8	10	11 (see note 14)	µs
T_{rr}	Register clock period (see note 14)	400	1000	N/A	ns
t_{rr}	Register clock pulse rise time	10	20	40	ns
t_{rf}	Register clock pulse fall time	10	20	40	ns
t_{or}	Register clock pulse edge overlap	TBD	50	70	ns
t_{wx}	Reset pulse width (see note 15)	>3 t_{rx}	60	100	ns
t_{rx}	Reset pulse rise time	TBD	10	30	ns
t_{fx}	Reset pulse fall time	TBD	10	30	ns
t_{dx}	Delay time, ØR off to RØ2 falling	10	30	50	ns
t_{drg}	Delay time, RØ2/RØ3 falling to DG falling	TBD	20	N/A	µs
t_{dgr}	Delay time, DG falling to RØ2/RØ3 rising	TBD	20	N/A	µs

NOTES

13. Generally $T_i = t_{drt} + 7t_{oi} + t_{dtr}$.
14. As set by the system specifications.
15. The RØ2 pulse width is normally minimised, as shown, such that the RØ1 and RØ3 pulse widths can be increased to maximise the output reset and signal sampling intervals.

DEFINITIONS

Back-thinning

A back-thinned CCD is fabricated on the front surface of the silicon and is subsequently processed for illumination from the reverse side. This avoids loss of transmission in the electrode layer (particularly significant at shorter wavelengths or with low energy X-rays). This process requires the silicon to be reduced to a thin layer by a combination of chemical and mechanical means. The surface is "passivated" and an anti-reflection coating may be added.

AR coating

Anti-reflection coatings are normally applied to the back illuminated CCD to further improve the quantum efficiency. Standard coatings optimise the response in the visible, ultra-violet or infra-red regions. For X-ray detection an uncoated device may be preferable.

Read-out noise

Read-out noise is the random noise from the CCD output stage in the absence of signal. This noise introduces a random fluctuation in the output voltage that is superimposed on the detected signal.

The method of measurement involves reverse-clocking the register and determining the standard deviation of the output fluctuations, and then converting the result to an equivalent number of electrons using the known amplifier responsivity.

Dummy output

Each output has an associated "dummy" circuit on-chip, which is of identical design to the "real" circuit but receives no signal charge. The dummy output should have the same levels of clock feed-through, and can thus be used to suppress the similar component in the "real" signal output by means of a differential pre-amplifier. The penalty is that the noise is increased by a factor of $\sqrt{2}$. If not required the dummy outputs may be powered down.

Dark signal

This is the output signal of the device with zero illumination. This typically consists of electrons thermally generated within the semiconductor material, which are accumulated during signal integration. The dark signal is a strong function of temperature, as described in note 5.

Correlated Double Sampling

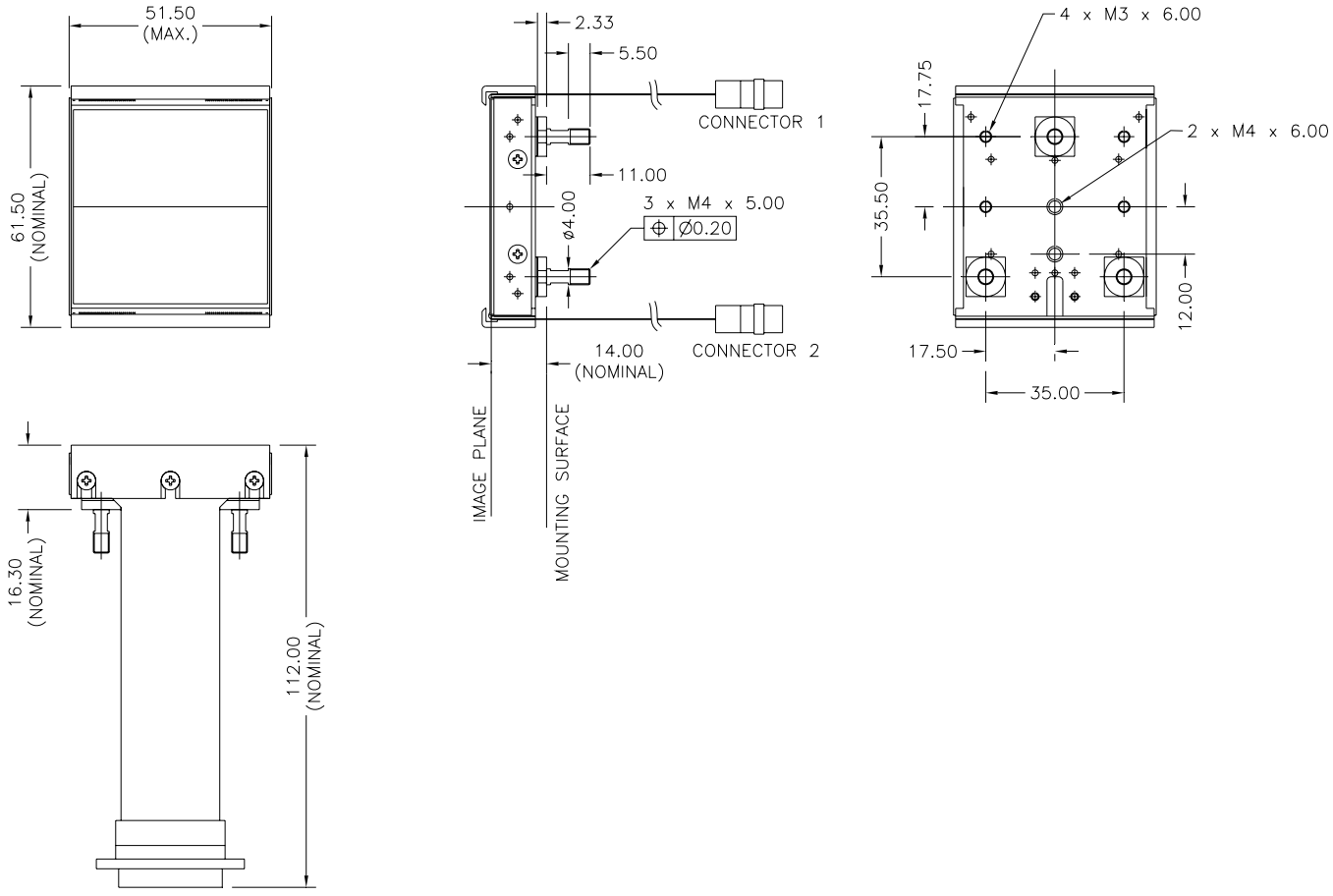
A technique for reducing the noise associated with the charge detection process by subtracting a first output sample taken just after reset from a second sample taken with charge present.

Charge Transfer Efficiency

The fraction of charge stored in a CCD element that is transferred to the adjacent element by a single clock cycle. The charge not transferred remains in the original element, possibly in trapping states and may possibly be released into later elements. The value of CTE is not constant but varies with signal size, temperature and clock frequency.

PACKAGE DETAIL

The side covers can be removed for close butting. Before removing the connector edge covers, consult e2v technologies.



HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. The sensor is shipped with shorting blocks attached to each micro D connector for electrostatic protection. These must be removed before use. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded
- Unattended CCDs should not be left without the shorting blocks connected.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (all CCD pins except V_{ss}, DD, RD, OD and OS) but not to the other pins.

The devices are also assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the surface of the CCD.

The device is vulnerable to edge damage in this buttable package, so handle with care.

For long-term storage we recommend keeping the sensors in a dry environment, eg the sealed shipping bags.

HIGH ENERGY RADIATION

Parameters may begin to change if the device is subject to a dose of ionising radiation greater than 10^4 rads. Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v technologies.

TEMPERATURE RANGE

Operating temperature range ..... 153 - 323 K
Storage temperature range ..... 143 - 373 K

Full performance is only guaranteed at the nominal operating temperature of 173K.

Operation or storage in humid conditions before cooling may give rise to ice on the sensor surface at low temperatures, causing irreversible damage.

Maximum rate of heating or cooling ..... 5 K/min

PART REFERENCES

CCD203-82-g-C60 Standard silicon, astro broadband
CCD203-82-g-C59 Deep depletion, basic midband
g = cosmetic grade