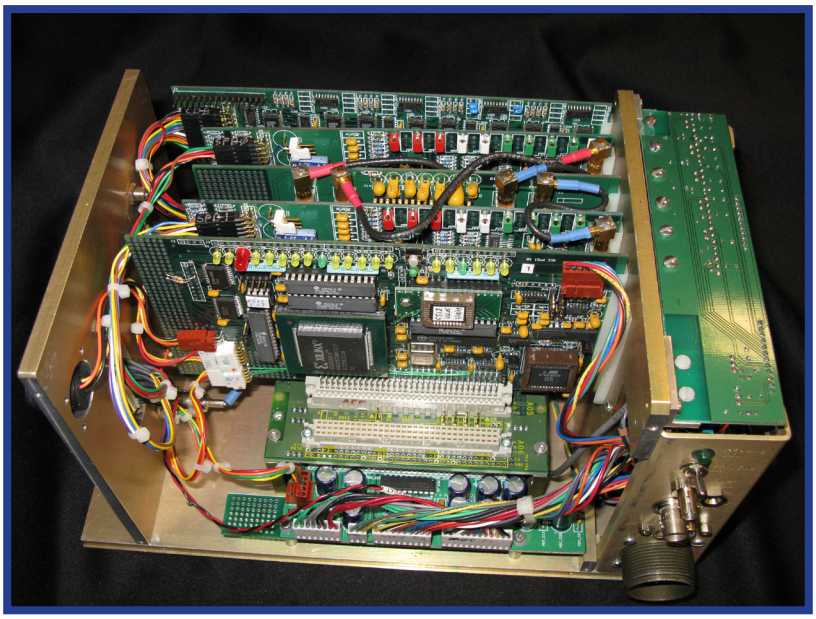
UCAM CCD Controller Hardware Manual

Mingzhi Wei

Richard Stover



Create on: September 04 2009
Last modified: January 7, 2011 3:08 PM

Revision 1.0

Table of Contents

List of Figures

List of Tables

Acknowledgments

Parts of this manual are derived from documentation produced by the Chinese Academy of Sciences National Astronomical Observatories LAMOST development team during their visit to UCO/Lick Observatory in 2008. Dr. Lei Jia produced most of that documentation.

1. Introduction

1.1. UCAM History

The UCAM controller was developed by Mingzhi Wei as part of the replacement of the first-generation UCO/Lick guide cameras. All of the original UCAM systems were guiders. In this role the controllers had a limited range of requirements. As the hardware developed it was realized that this new controller, capable of operating a CCD for a guider, could be made to operate most modern CCDs with only modest enhancements and that the same hardware that runs the guiders could also replace the aging Lick science-CCD controllers. As a result of this continued work the UCAM controller has replaced all CCD controllers on Mt. Hamilton. The controller has undergone a number of enhancements although the basic architecture and printed circuit board functions have remained the same. There have been new versions of some of the printed circuit boards, and the new versions take advantage of advances in component technologies or replace obsolete components. Both the new and old versions of these printed circuit boards are covered in this manual.

1.2. This Document

This document describes the current state of the ongoing evolution of the UCAM CCD controller. In the Section 2 we give a brief description of the major components that make up a typical UCAM controller system. In sections 3 through 6 we describe each of the major components in detail. In section 7 we describe the CCD temperature measurement and control system. Section 8 describes cabling details. Section 9 gives further details on the software that runs in the controller. Section 10 describes how to set up a new controller. Section 11 describes the voltages produced by the controller. Section 10 describes various diagnostic tests and Section 11 describes typical waveforms. COMPLETE AFTER DOCUMENT IS FINISHED

1.3. UCAM Design Philosophy

Some controllers are designed to be as general and non-specific as possible. They are somewhat like general-purpose waveform generators. The design of the UCAM controller has taken a different approach. We believe we know a lot about how CCDs work, having worked with dozens of types of CCDs over the last several decades. So instead of designing a CCD controller that knows nothing about CCDs, the UCAM controller is designed with an enormous amount of technical knowledge build into the hardware. This is made possible by the extensive use of programmable logic devices. These devices provide the designer with the generality of software combined with the speed and flexibility of hardware. The controller is run by programmable logic devices rather than a central CPU. The UCAM controller does has a small CPU but its function is one of communication and data translation. FOR THE MOST PART it is not involved directly in CCD operation.

By building CCD knowledge into the hardware, the specification for how the CCD is to operate becomes simpler. Waveform tables for the UCAM controller are usually much simpler than in a general purpose waveform generator style CCD controller. The generality of the programmable logic device allows us to add new capabilities as the need arises.

1.4. Other Documents

This manual is about the hardware. A separate document, *Operating the UCO/Lick UCAM CCD Controller*, is available for controller users who wish to write software that communicates with the

controller.

2. Hardware Overview

The size, shape, and mounting details of the standard UCAM controller enclosure were designed to be a direct replacement for the original Lick guide cameras. A totally different enclosure is possible but at Lick we have not found that to be necessary.

Electronically the controller is designed around Xilinx FPGAs. These programmable logic devices provide all of the precise timing for operation of the CCD. A small microprocessor is used for communications with the control computer and for defining register values that control the Xilinx operation, but the microprocessor takes little direct part in running the CCD. In fact the microprocessor is put to sleep during CCD readout to avoid introducing noise.

2.1. Electronic Hardware Groups

The controller electronics consists of five primary groups of related hardware as illustrated in Figure 1. The five primary groups are the controller electronics, the CCD temperature control system, the power supply, the dewar interface, and the computer interface. As suggested in the Figure, the CCD controller and temperature control system are usually housed in the same enclosure in the UCO/Lick designs.

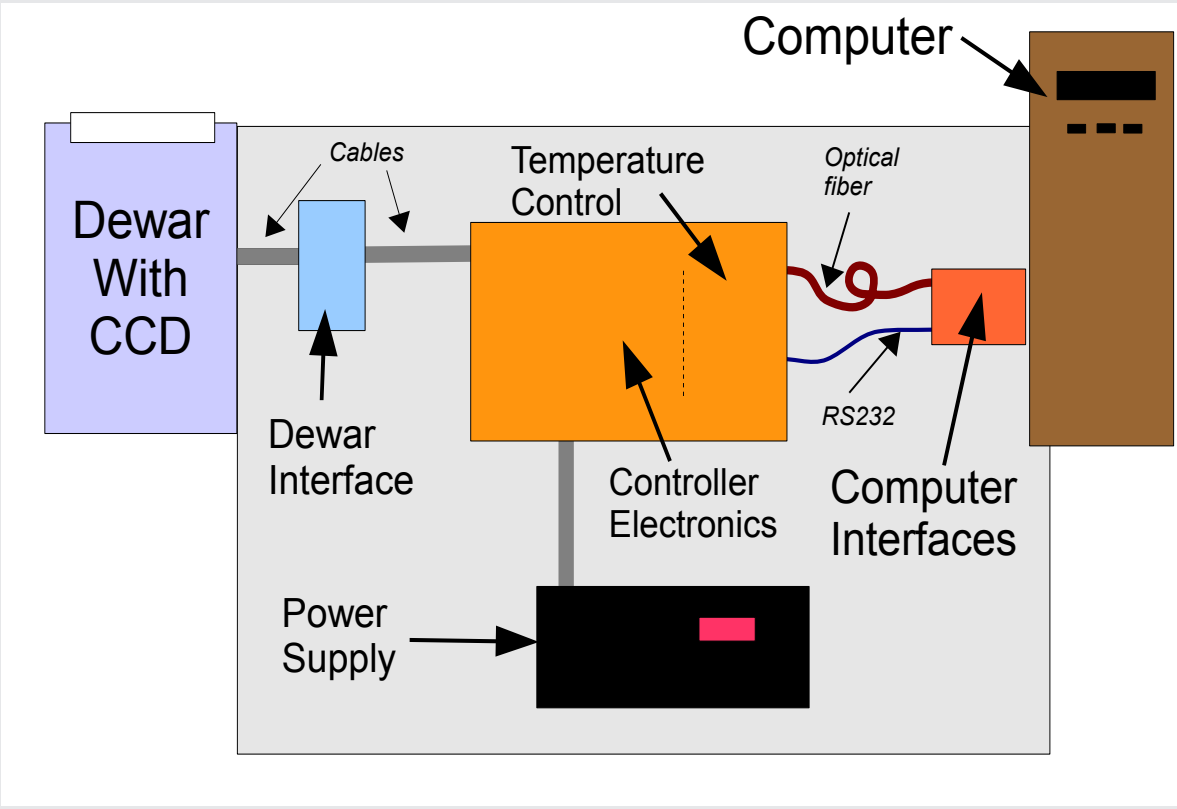


Figure 1. The typical UCAM controller.

In this chapter we give a brief description of the general physical appearance of the five major groups. Each group will be covered in detail in later sections.

2.2. Controller Electronics

The controller electronics generates all of the bias voltages and clock waveforms needed to run a CCD. It also performs signal processing and digitization of the video output from the CCD. The digital data are sent over a fiber optic cable to a receiving computer.

The controller electronics is typically contained in an enclosure as show in Figure 2. The controller in Figure 2 was built for the Automatic Planet Finding (APF) telescope on Mt. Hamilton. The connectors visible on the left-end bulkhead of the enclosure consist of DB25 and DB37 connects, two 50-ohm coax connectors, and an 8-pin digital I/O connector. The connectors cable to the dewar interface electronics of the APF CCD dewar. These connectors are customized to meet the needs of individual dewars/CCDs and in the case of the guiders the connectors are dispensed with altogether and the small guider CCD housing is mounted directly on the controller bulkhead.

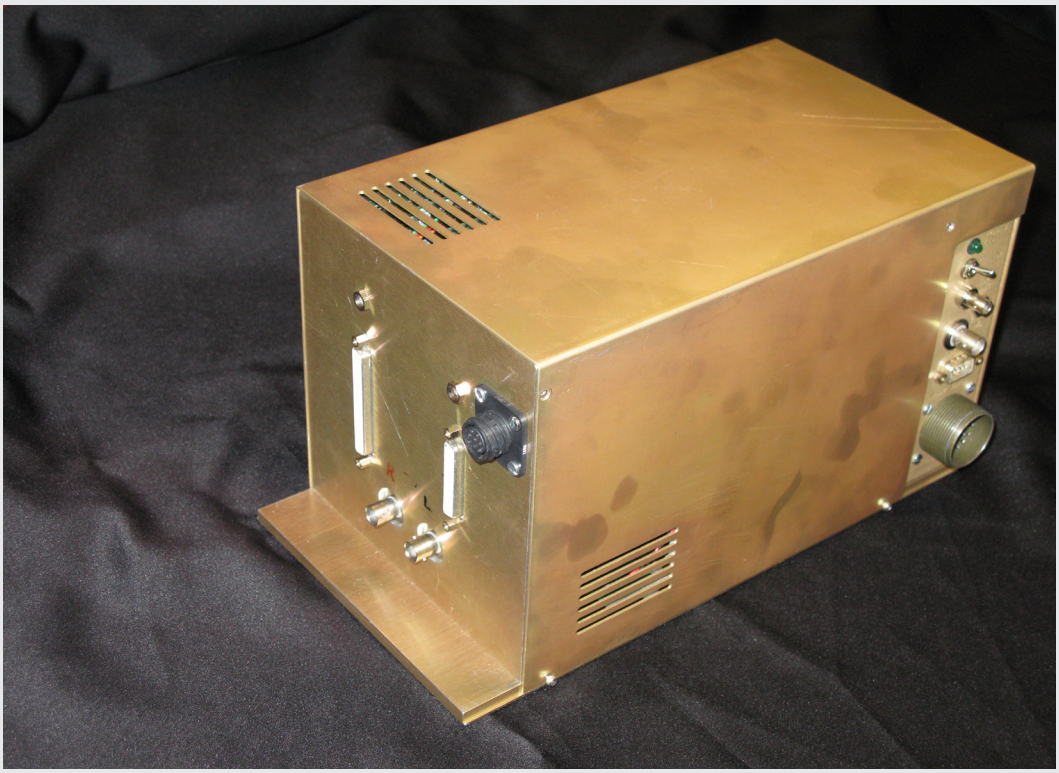


Figure 2. A typical UCAM controller enclosure. Many of the connectors are visible in this view.

The connectors on the right side include (from the bottom to the top) a large 17-pin power connector, a DB9 RS232 connector, a BNC coax connector (shutter control output), and an optical fiber connector (image data output). Above these is a toggle switch, and a green LED. The RS232 connector is cabled to either a computer interface or directly to a computer RS232 serial port, depending on the particular hardware configuration. All commands which control the operation of the UCAM hardware are communicated over this RS232 connection. The single fiber optic output is used to send digital image data to the computer that captures, processes, or stores image data. The toggle switch controls all of the LEDS including the green LED on the enclosure and the LEDs on some of the internal electronics boards.

Figure 3 shows the typical guider (with the cover removed). The DB25 and DB37 connectors seen in Figure 2 are eliminated and instead the CCD and its housing are mounted directly onto the bulkhead of the UCAM controller electronics housing. Also note that the power supply and other connectors at the far right side (as seen in Figure 2) are not visible. They have been rotated 90 degrees to the back of the controller housing and are out of sight in this view. This alternate placement of the connectors gives us greater flexibility for the routing of cables to and from the controller.

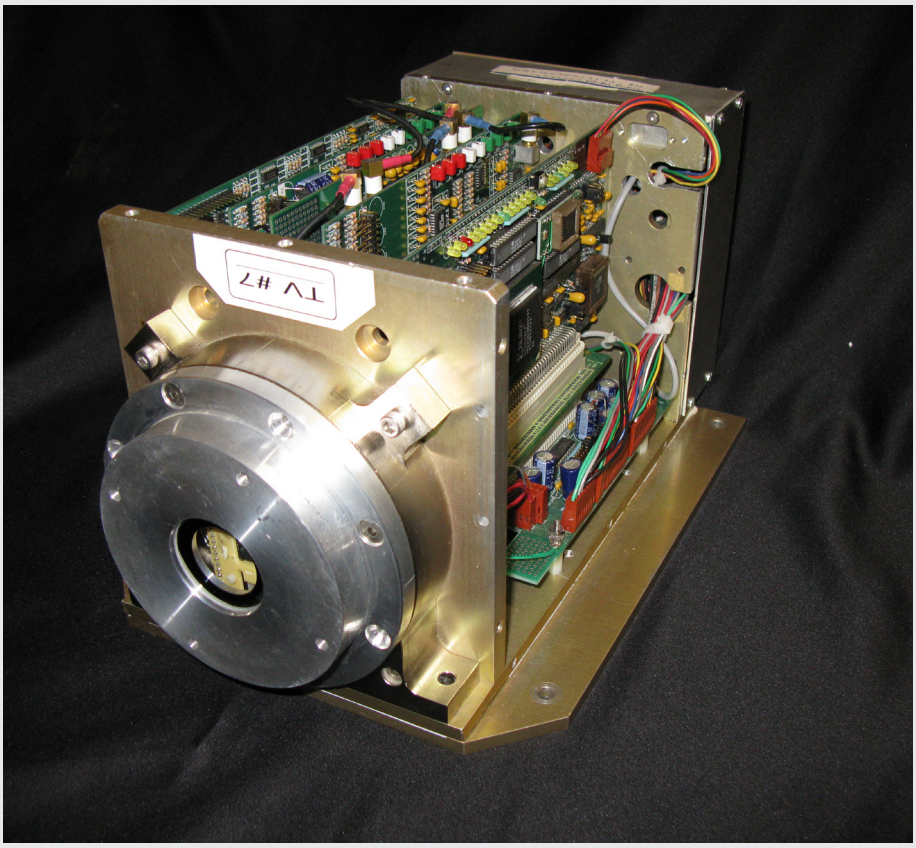


Figure 3. A typical guider with the thermoelectrically-cooled CCD and its housing mounted directly on the bulkhead of the UCAM controller.

As illustrated in Figure 3 the controller electronics consists of a number of printed circuit boards which are plugged into a common backplane. Most wiring between the boards passes over this backplane. There are a number of small coax cables that run between some of the boards to carry the high-level analog signal from the Signal Processing Board to the analog-to-digital converter (ADC) board. These details are discussed further in Sections 3.5 and 3.6 (starting on page 24).

2.3. Temperature Control System

The CCD temperature control system consists of a printed circuit Temperature Control Board (TCB) and a local power regulator board and these boards are housed in the compartment at the back of the CCD controller enclosure. This compartment is shown in Figure 4. The compartment is somewhat crowded because in addition to the TCB there are local voltage regulator boards for both the temperature control system and for the CCD controller electronics. The voltage regulators are described in more detail in Section 8.1 on page 37.

The temperature control system is electrically isolated from the CCD controller electronics. The

systems use separate power supplies and the RS232 communications link between the two systems is opto-isolated. This electrical isolation allows the temperature control system to run continuously and asynchronously with respect to the CCD control electronics without introducing noise into the CCD readout.

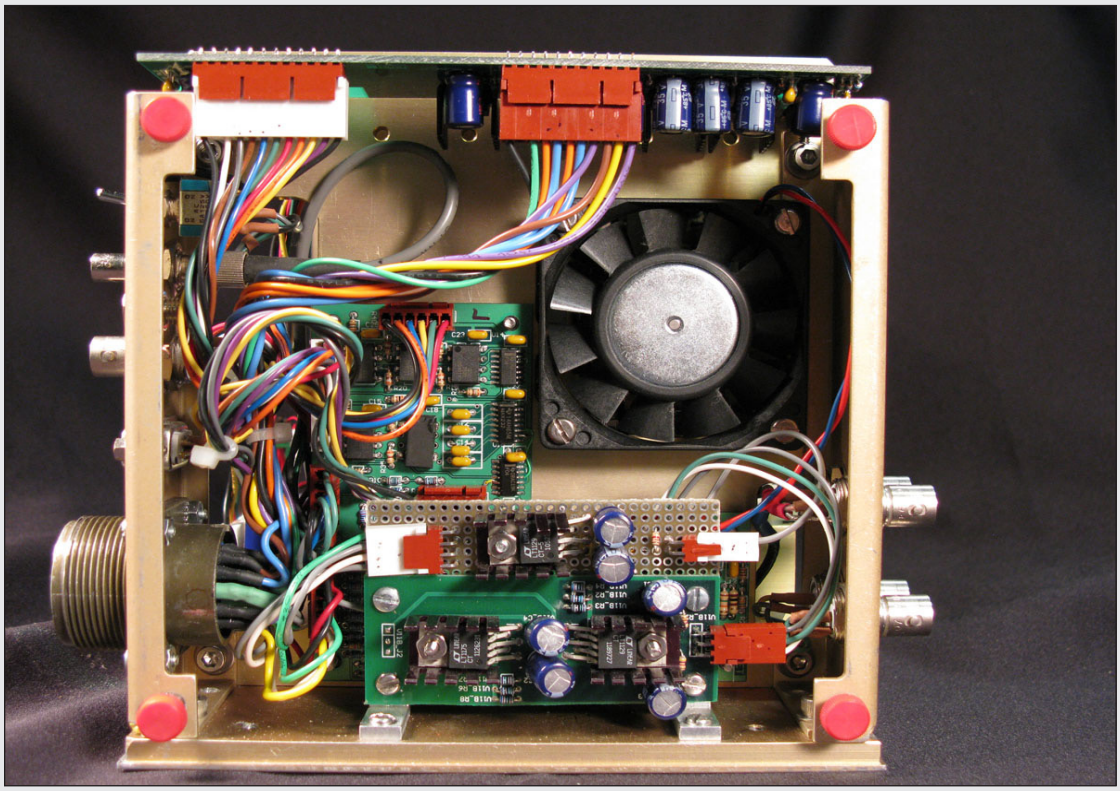


Figure 4. The compartment with the CCD temperature control system and local voltage regulators.

2.4. Power Supply

The power supply is housed in a 19-inch rack-mountable chassis as shown in Figure 5. The AC power is controlled with the power switch. The CCD on-chip amplifier voltage (the “high voltage”) is controllable with separate push buttons. The CCD temperature is displayed in a small panel meter. The LED and panel meter brightness is controlled with a potentiometer and can be turned off.

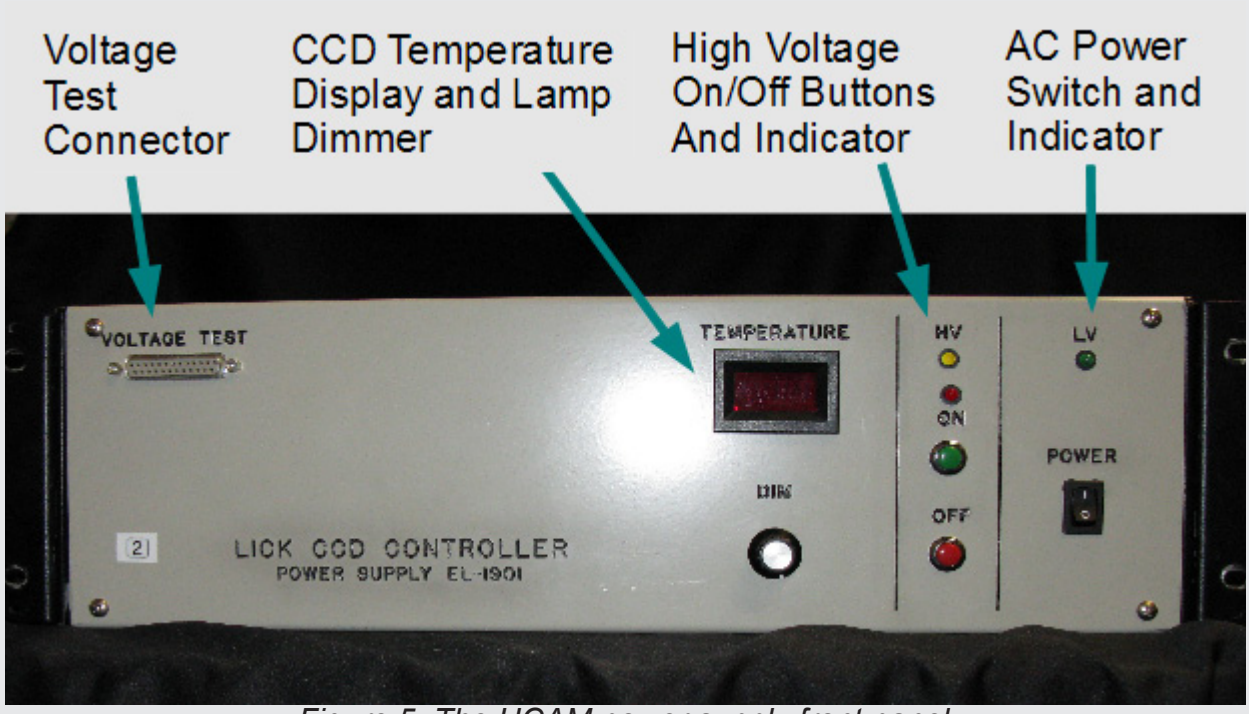


Figure 5. The UCAM power supply front panel.

The power supply is connected to the UCAM controller through a 17-pin power cable. That cable attaches to the connector on the back-side panel of the power supply, which is shown in Figure 6. Also note the 5V sense input, a BNC connector. When this sense feedback is used the power supply can adjust the output of the main 5V supply to overcome resistive voltage drops in the 17-pin power cable. The voltage adjustment capability of the sense feedback is only about 0.2V, so it will not compensate for the voltage drop in a long power supply cable. Also note the ground plug. A wire attached to the power cable shield is plugged into this connector. The actual position of the sense feedback and ground plug may vary from that shown in the Figure 6.

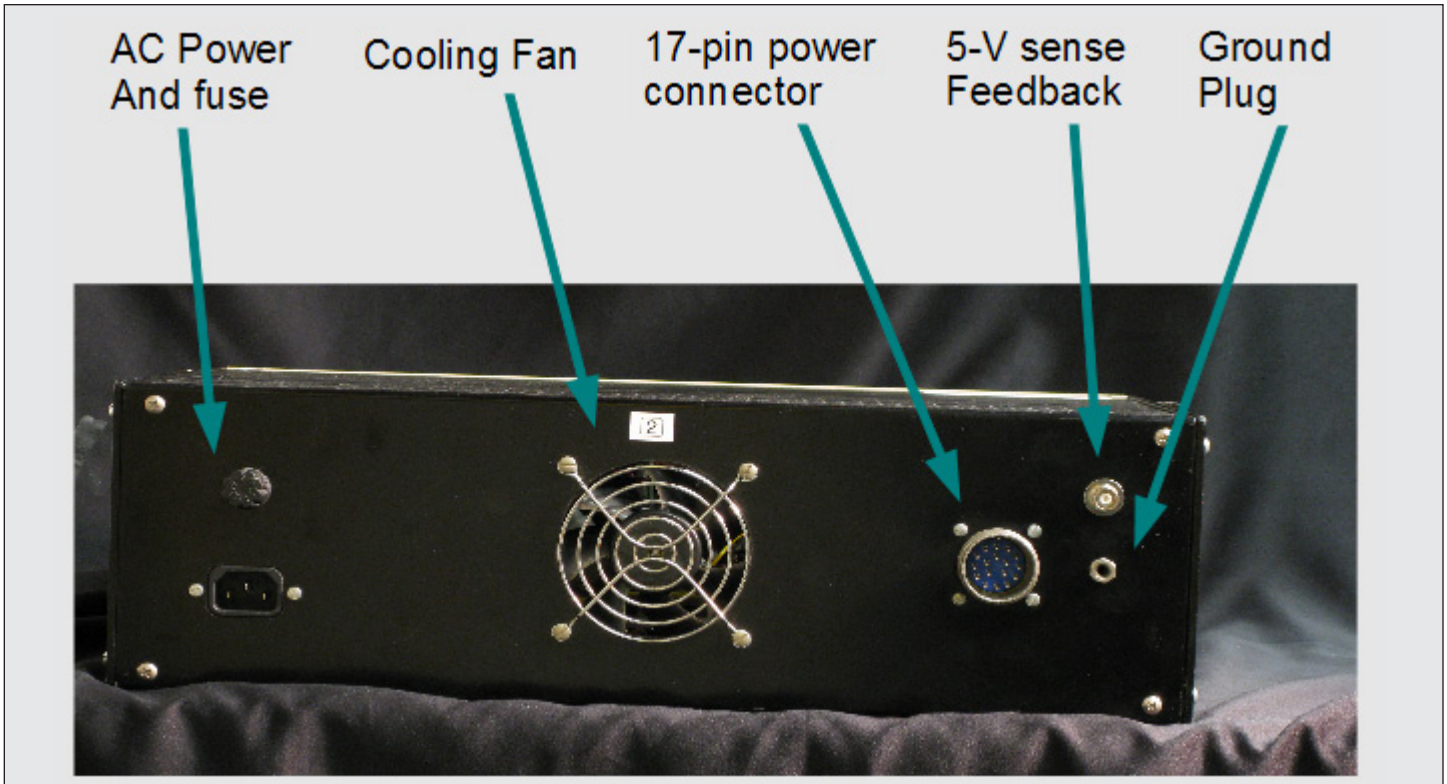


Figure 6. The UCAM power supply backside showing the AC input, 17-pin DC output, 5V sense input, and ground plug.

2.5. Dewar Interface

The dewar interface is not used for the guiders because the guider CCD is mounted directly to the controller. But for all science CCDs which have independent dewars the interface houses one or more preamplifier/interconnect boards. Each board provides a dual channel preamplifier for the video outputs from the CCD and the necessary interconnect cabling for connecting the UCAM controller to the specific CCD dewar. The exact details of the interconnect cabling depends on the CCD and dewar. The interconnect board also provides additional bias voltage filtering plus analog switches and relays that allow the controller to disconnect the voltages and clocks from the CCD.

An example of the dewar interface built for the Automatic Planet Finding CCD and dewar is shown in Figure 7. The PC board shown in this Figure is the standard board used for UCO/Lick science CCDs and this board will be described in detail in § 5, ”Dewar Interface Components”, on page 34.

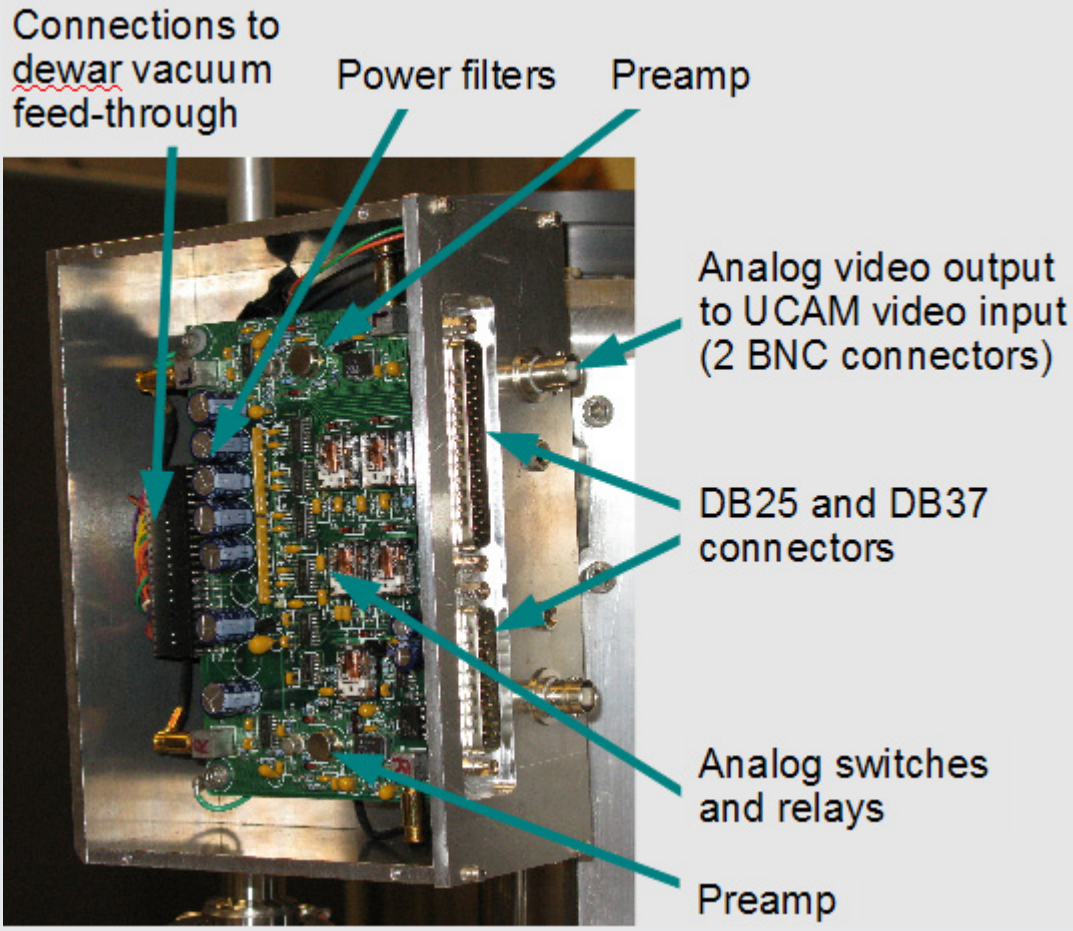


Figure 7. The dewar interface built for the APF CCD. Major sections of the interconnect board are labeled along with most of the external connectors.

2.6. Computer Interface

Digital image data are sent to the image-capture computer over a fiber optic cable. We have two options for interfacing the fiber optic cable to the computer. Those options are shown in Figure 8 and Figure 9.

Figure 8 shows the PCI bus interface. This was the original interface designed for the UCAM controller. The particular PCI interface shown in Figure 8 has three fiber optic connectors because this board is designed to function with the older San Diego State University CCD controllers (known now as Astronomical Research Cameras, Inc.). Our more recent PCI interfaces have just one fiber connector to work with the UCAM controller. While the PCI interface is still available and it is in use at Mt. Hamilton the preferred interface for new computers is the USB interface show in Figure 9.

The USB interface is a stand-along box powered by a small wall-mount power supply. The USB interface provides connections for both the data optical fiber and an RS232 serial port.

Linux device drives have been written for both the PCI and USB interfaces and they present the same device interface and protocols to upper-level software.

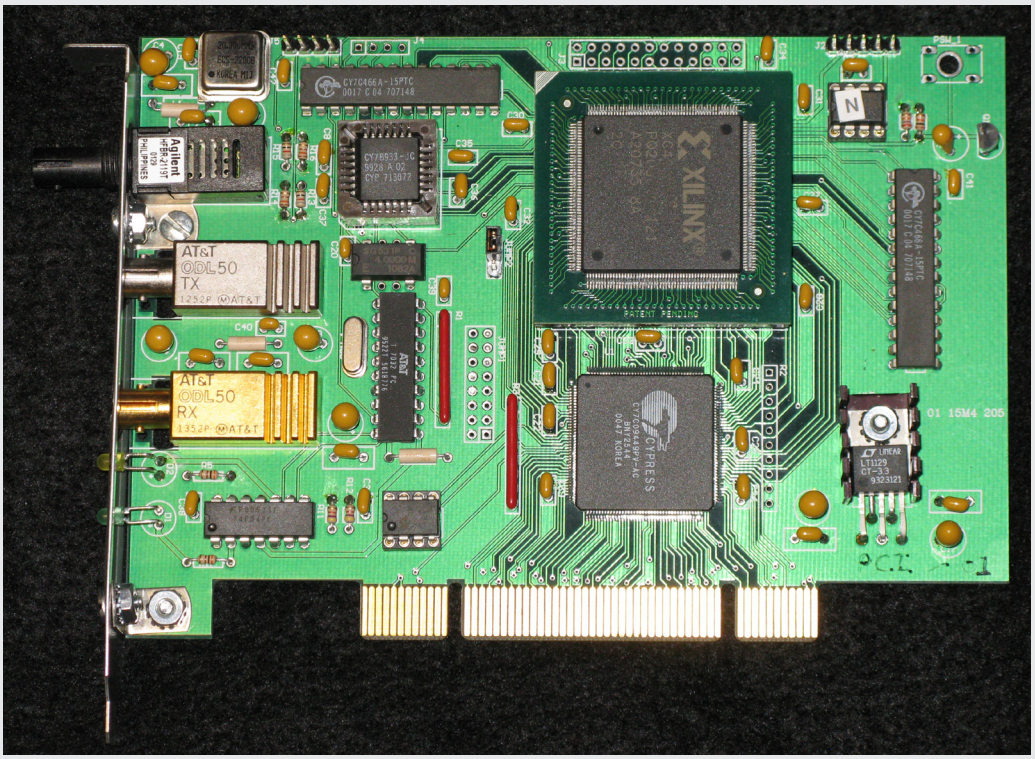


Figure 8. The UCAM PCI interface. This can be used in any PCI-bus computer.

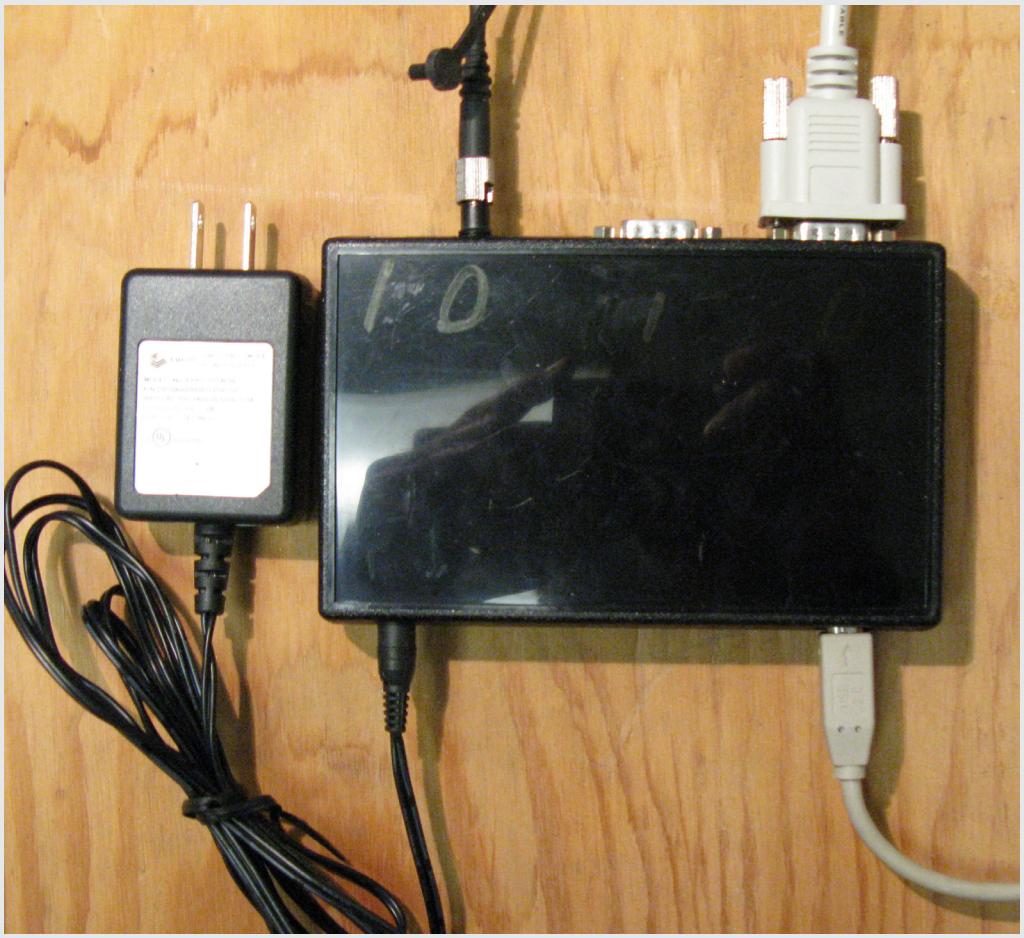


Figure 9. The UCAM USB interface is a stand-alone interface box.

The control computer can send commands to the UCAM controller to set and read back a wide variety of parameter values. The UCAM controller also sends event messages, which announce when important events occur. Typical events include, “Erase begun”, “Shutter open”, “Readout complete” and more. All of this communication activity occurs over a single UCAM RS232 serial I/O port. The UCAM serial line can connect to any serial port available to the control computer. This can be a serial port built into the computer, a USB-attached serial port, or the serial port provided by the UCAM fiber USB computer interface.

3. CCD Controller Components

The controller shown in Figure 2 on page 4 and Figure 3 on page 5 is divided into two compartments. The controller electronics is located in the larger, forward compartment as shown in Figure 3. The rear compartment houses the temperature control electronics, some local voltage regulators, and a fan. All of the printed circuit boards in the controller compartment plug into a backplane. The backplane carries power supply voltages and digital control signals.

3.1. Overview

The controller electronics consists of a series of printed circuit boards that plug into a common backplane. That backplane carries power supply voltages to all of the boards and digital signals between boards. The controller printed circuit boards are listed in Table 1. Older systems use the SPB, CDB, and ADC boards while the newest systems use the DSPB, QADC, and NCDB boards. In the following subsections we will describe each of these items in detail. We begin with a detailed description of the backplane.

Board Name	Board Abbreviation	Number of Boards	Functions
Timing Control	TIM	1	Communicate with control computer, control Xilinx operation, control programmable voltage levels, read-back of voltages.
Signal Processing	SPB	1 or 2	Produce bias voltages for CCD on-chip amplifiers and CDS video processing (correlated double sampling) of CCD video output.
Dual Signal Processing	DSPB	1 to 8	Produce bias voltages for CCD on-chip amplifiers and two channels of CDS processing of CCD video output.
Dual ADC	ADC	1	Two channels of analog-to-digital conversion of the processed video signal from the SPB or DSPB and transmission to the image capture computer.
Quad ADC	QADC	1 to 4	Four channels of analog-to-digital conversion of the processed video signal from the SPB or DSPB and transmission to the image capture computer.
Clock Driver	CDB	1	D-to-A converters define the high and low voltages for CCD clocks. Under Xilinx control generates all clocked waveforms for the CCD using parameters supplied from the TIM CPU.
New Clock Driver	NCDB	1 to 8	D-to-A converters define the high and low voltages for CCD clocks. Under Xilinx control generates all clocked waveforms for the CCD using parameters supplied from the TIM CPU.

Table 1. CCD controller printed circuit boards.

The minimum UCAM system consists of four circuit boards: one TIM, one SPB or DSPB, one CDB or NCDB, and one ADC or QADC. The maximum UCAM system consists of twenty one circuit boards: one TIM, eight DSPBs, four QADCs, and eight NCDBs.

3.2. Backplane

The backplane is shown in Figure 10. This Figure shows the same controller as in Figure 3, page 5, with all of the circuit boards removed. The backplane consists of a commercial 6-position VMEbus backplane and a power interconnect board. The interconnect board plugs into the pins of the first VMEbus connector. Although we are using VMEbus hardware the pin definitions are UCAM-specific. They are not traditional VMEbus pin definitions. The pin definitions are given in Appendix B, on page 58.

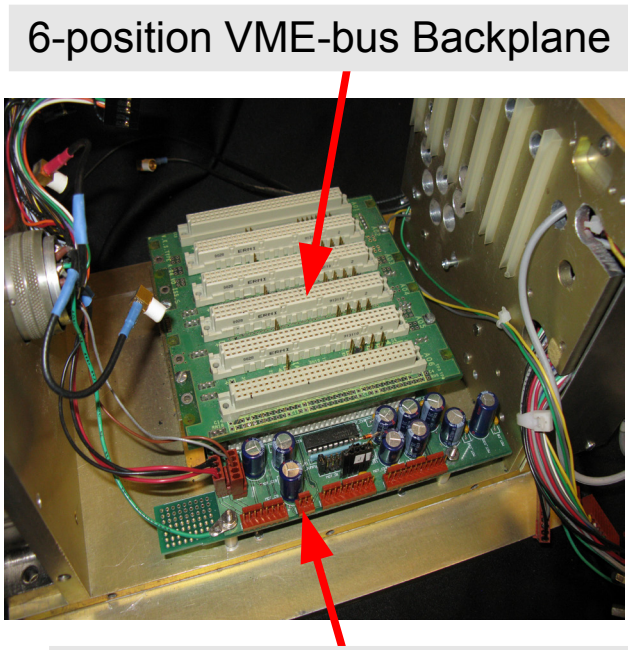


Figure 10. The UCAM controller uses a commercial VMEbus backplane. A small interconnect board provides power supply connections and filtering as well as other connections.

The power interconnect board employs Molex-style connectors. The row of four connectors (along the bottom of the board in Figure 10) all connect to power supply cables. In this Figure all those cables have been removed. Some of these connectors can be used as voltage test points. The details are given in Section 8.4 on page 41. Two additional connectors are located near the left edge of the board and in Figure 10 the cables are still connected. The cable with the black and red wires provides power (5 to 7 V) to the thermoelectric cooler of the Lick guider and the connector with the blue and brown wires carries the input signals from the CCD temperature sensing diode and power for the temperature control heater resistor. (The guider runs as cold as possible so there are only the temperature sense wires seen guider backplane in Figure 10.) The capacitors on the interconnect board provide local filtering for all power supply voltages.

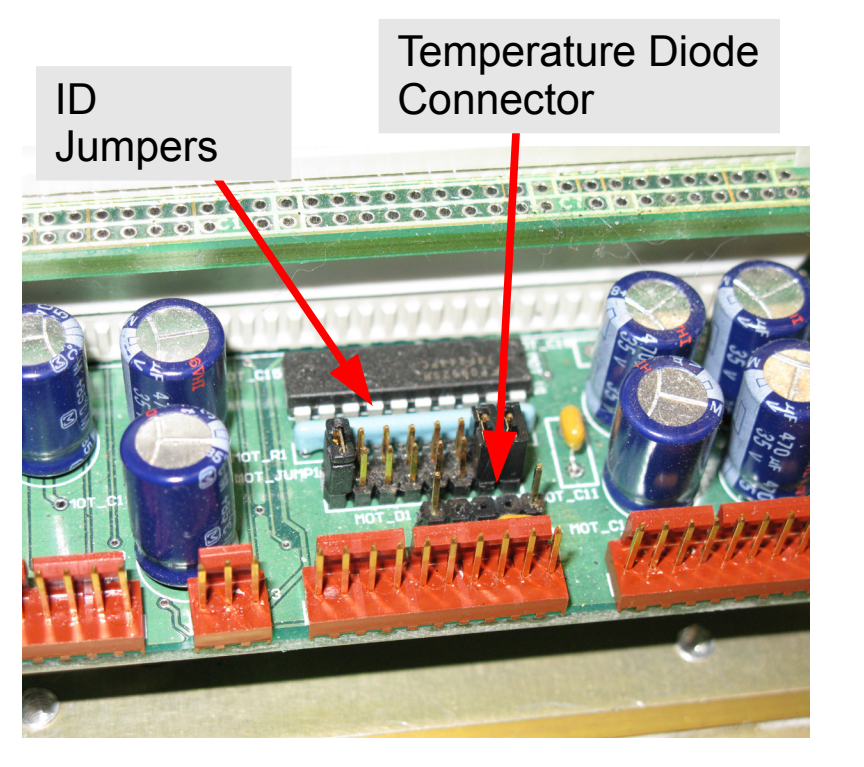


Figure 11. The camera ID jumpers and the local temperature diode connector are on the power interconnect board.

In addition to the power connectors the interconnect board has a set of eight jumpers and one additional connector, as shown in the close-up in Figure 11 above. The eight jumpers define an 8-bit camera configuration number and the currently defined numbers are show in Table 2. Each configuration number defines a unique set of waveforms and voltages which the controller will generate. When the controller is first powered up the CPU on the TIM reads the configuration number from the jumpers and sets up all of the voltages and waveforms for that configuration using parameters stored in its own nonvolatile memory. In addition to the configuration numbers shown in Table 2 the hex number **ff** has a special meaning. When the TIM reads this value it then reads its actual ID and all of the voltage and waveform parameters from a serial eprom associated with the CCD dewar. In this way the configuration of the controller is defined by the CCD it is connected to, not by the controller itself. The serial eprom is described in detail in § 11 on page 43.

Camera ID (hex)	Configuration
02	Lick test dewar with Loral 2kx2k CCD
03	Lick Camera with Fairchild 4kx4k CCD
04	Lincoln CCID20
05	APF Camera with e2v 2kx4k 42-90 CCD
06	SAO Camera with Site 2kx2k CCD
08	Dewar #7 with CCID56a/b CCD
0a	BAO Camera with Kodak CCD
0b	Lick dewar9 with Reticon 400x1200 CCD
0c	KAST RED RET400x1200
13	KAST Blue CCD3041
15	216 BFOS
17	New UCAM with e2v 4kx4k CCD
42	Lick UCAM with Loral 2kx2k ccd use DSPB
81	Prober camera with LBNL 2Kx4K CCD
82	Dewar #8 with LBNL 2kx2kCCD
83	Lick Guide Camera #2 with LBNL 400x690 CCD
84	Lick CCD Controller with LBNL SNAP CCD
86	Lick Camera with LBNL SNAP 3514(R)x3508(C) CCD
87	Lick Guide Camera with LBNL 470x1264 CCD
89	KAST Camera with LBNL CCD 1980x800
93	Lick Guide Camera #3 with LBNL 400x690 CCD
a3	Lick Guide Camera #4 with LBNL 400x690 CCD
b3	Lick Guide Camera #5 with LBNL 400x690 CCD
c3	Lick Guide Camera #6 with LBNL 400x690 CCD
d3	Lick Guide Camera #7 with LBNL 400x690 CCD
e3	Lick Guide Camera #8 with LBNL 400x690 CCD
f3	Lick Guide Camera #9 with LBNL 400x690 CCD

Table 2. Currently defined camera configuration ID numbers.

The most significant bit of the ID number is the left-most jumper as shown in Figure 11. The jumpers in the Figure would be read by the TIM CPU as hex 83, Lick Guide Camera #2.

The other connector as shown in Figure 11 is labeled *Temperature Diode Connector*. A calibrated diode is connected between the two pins of the connector. On some controllers the missing three pins of the temperature diode connector in Figure 11 are still there, but they are unused – the diode connects between the end pins. Note: This diode must be in place for the CCD temperature-sense diode to work properly. The cathode (the end of the diode with the black band) attaches to the left-most pin.

3.3. Timing and Control Overview (TIM)

Since its original design the TIM printed circuit board has undergone a major revision to take advantage of faster, lower power 3.3V digital logic devices and to replace some obsolete components in the design. As a result there are two versions of the TIM. For identification purposes these two versions are shown together in Figure 12. The version number is located in the circuit board silk screen near the lower right edge of the boards.

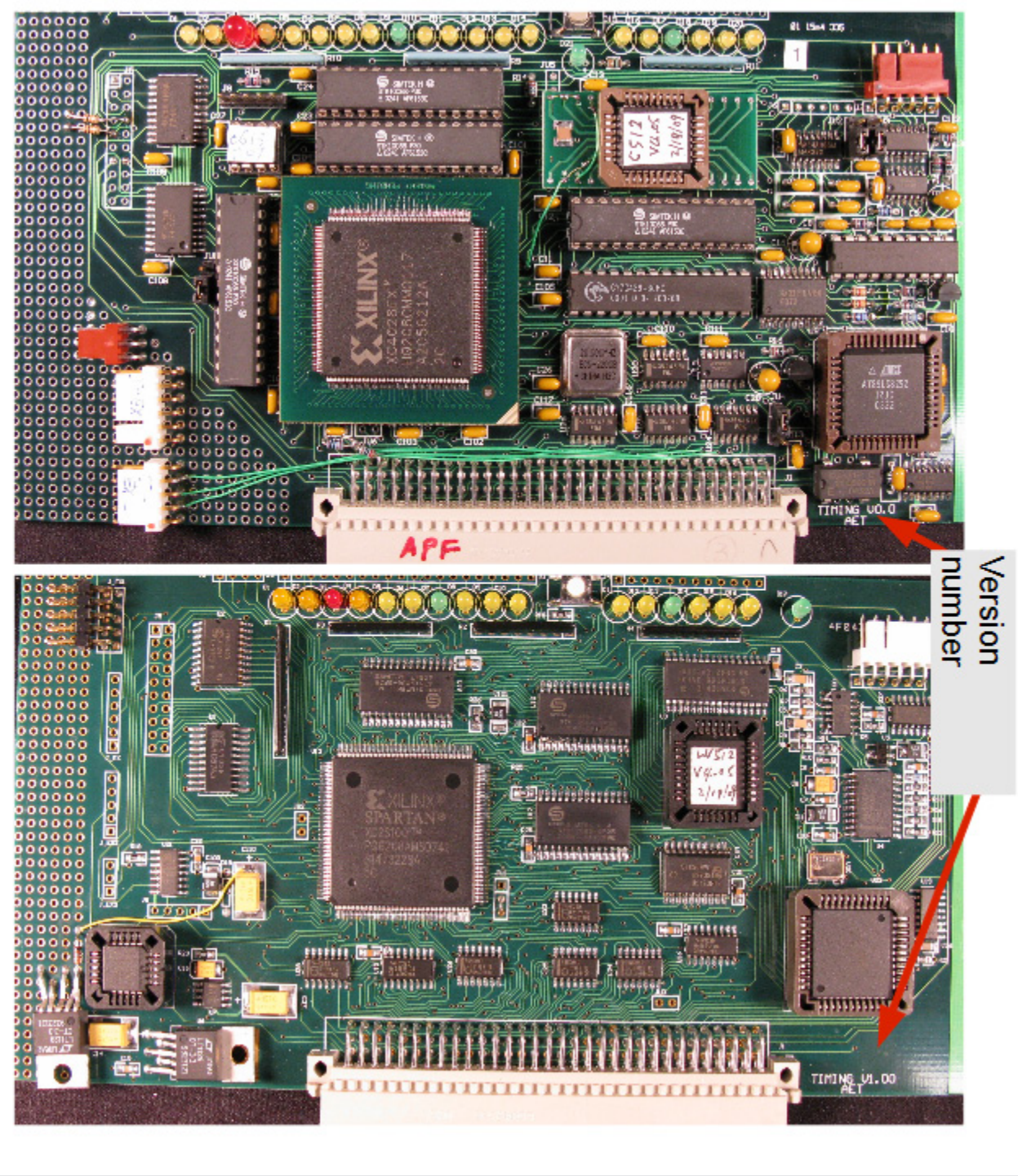


Figure 12. TIM version 0 is shown at the top and version 1 is shown at the bottom.

Although the layout of the boards is not identical there are some general features in common. Near the center of the board is a large Xilinx FPGA. Across the top of the board is a set of red, yellow, or green state indicator LEDs and a reset button. Along the left edge of the board is a general-purpose grid of 0.1-inch spaced holes. As seen in Figure 12 we have used that area for some modifications.

3.3.1. TIM Version 0

The Timing Control Board Version 0 is shown in more detail in Figure 13. This is the version of the

TIM in most of the UCO/Lick systems produced prior to 2009. The board shown in Figure 13 has one modification to make it compatible with Version 1. The small socketed integrated circuit identified as CPU program memory is mounted on a small daughter board which is plugged into the location of an earlier (now obsolete) eprom.

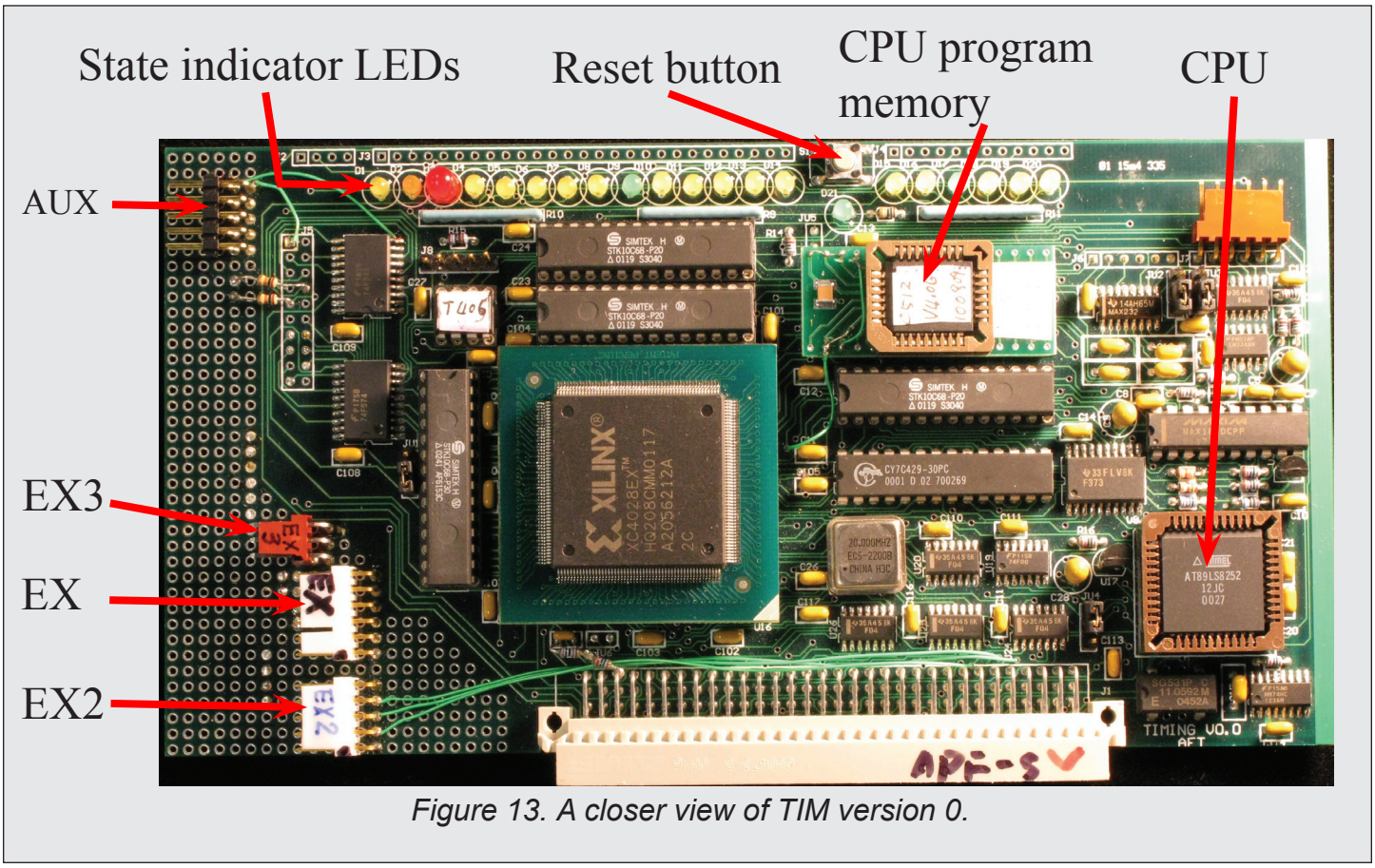


Figure 13. A closer view of TIM version 0.

This particular TIM has some extra connectors mounted in the general purpose area of the board. The connectors are labeled AUX, EX, EX2, and EX3 in the Figure. These connectors are not always present on all TIM boards. The AUX connector shares pins with the EX and EX2 connectors and the AUX connector is used when ribbon cable is used for the cable between the UCAM internal boards and the connectors on the UCAM bulkhead. If individual wire connectors are used (the original design) then the EX and EX2 connectors are used.

The definition of the AUX connector is shown in Figure 14 and the definitions of the three EX, EX2, and EX3 connectors is shown in Figure 15. The EX and EX2 connectors share some signals with the AUX connector. The EX3 connector provides two digital input bits which are often used for sensing shutter state.

Pin #	Bias Voltage
1	Digital Ground
2	V_{cc}
3	No connection
4	No connection
5	No connection
6	$\overline{ENV}$
7	DI (serial eprom)
8	DO (serial eprom)
9	SCK (serial eprom)
10	$\overline{CS}$ (serial eprom)

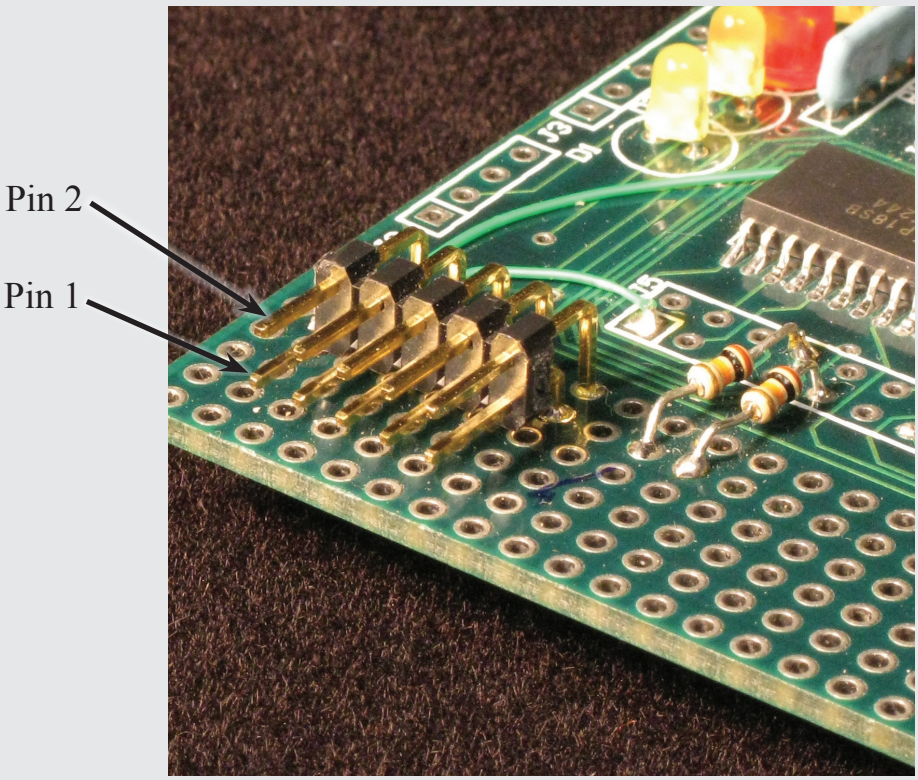


Figure 14. The AUX connector on the TIM0 board. This connector shares some signals with the EX and EX2 connectors.

Pin #	Function
EX-1	V_{cc}
EX-2	No connection
EX-3	No connection
EX-4	$\overline{ENV}$
EX-5	Digital Ground
EX-6	No connection
EX2-1	$\overline{CS}$ (serial eprom)
EX2-2	SCK (serial eprom)
EX2-3	DO (serial eprom)
EX2-4	DI (serial eprom)
EX2-5	No connection
EX3-1	Digital bit 0 (IN)
EX3-2	Digital bit 1 (IN)
EX3-3	Digital Ground

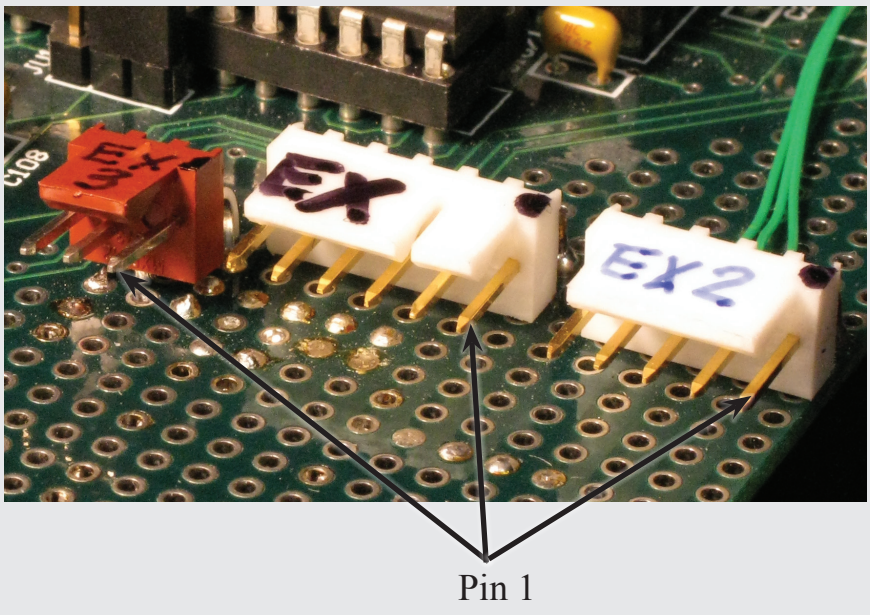


Figure 15. The three EX connectors on the TIM version 0 board. The EX and EX2 connectors share some signals with the AUX connector. The EX3 connector provides two digital input bits which are often used for sensing shutter state.

The state indicator LEDs and pins of the TIM connectors are defined in Figure 16. Note that above each LED is a test point. These points can be used to trigger an oscilloscope on any of the states.

The TIM receives commands and sends responses and messages over its RS232 serial port. To avoid noise from ground loops and other sources this port is not connected directly to the serial cable that runs back to the user's computer. Instead the lines of the RS232 serial port are connected via opto-isolators to a serial port on the CPU that runs in the temperature control system (see Section 7 on page 35). The temperature control CPU has a second serial port and that port connects to the cable that runs back to the user's computer. Incoming messages from the user's computer go to both the temperature control CPU and the TIM. They both recognize messages for themselves and ignore messages meant for the other CPU. Likewise, anything the temperature control CPU receives from the TIM is combined with any of its own messages and is forwarded to the second serial port where it is sent to the user's computer. The logic is shown schematically in Figure 17.

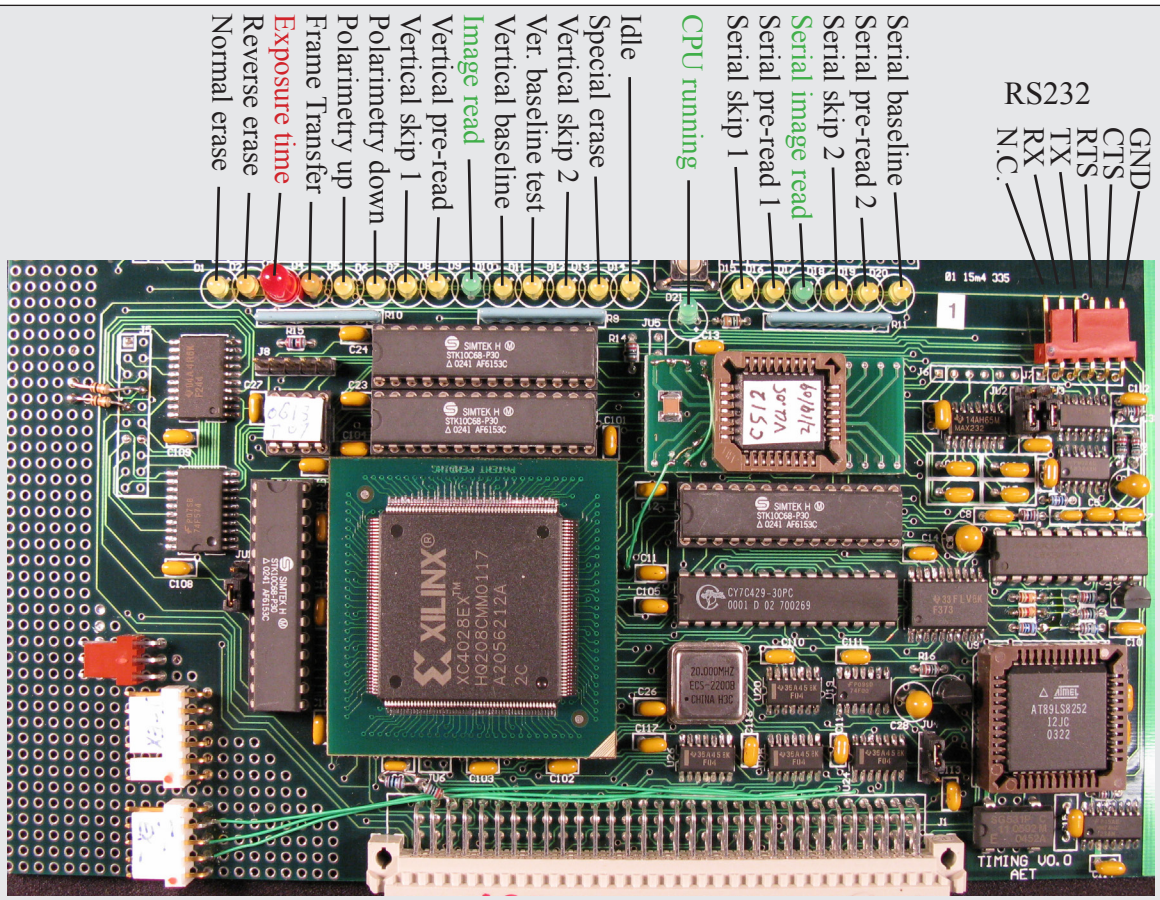


Figure 16. The state indicator LEDs and the connector pins of the TIM version 0 are defined.

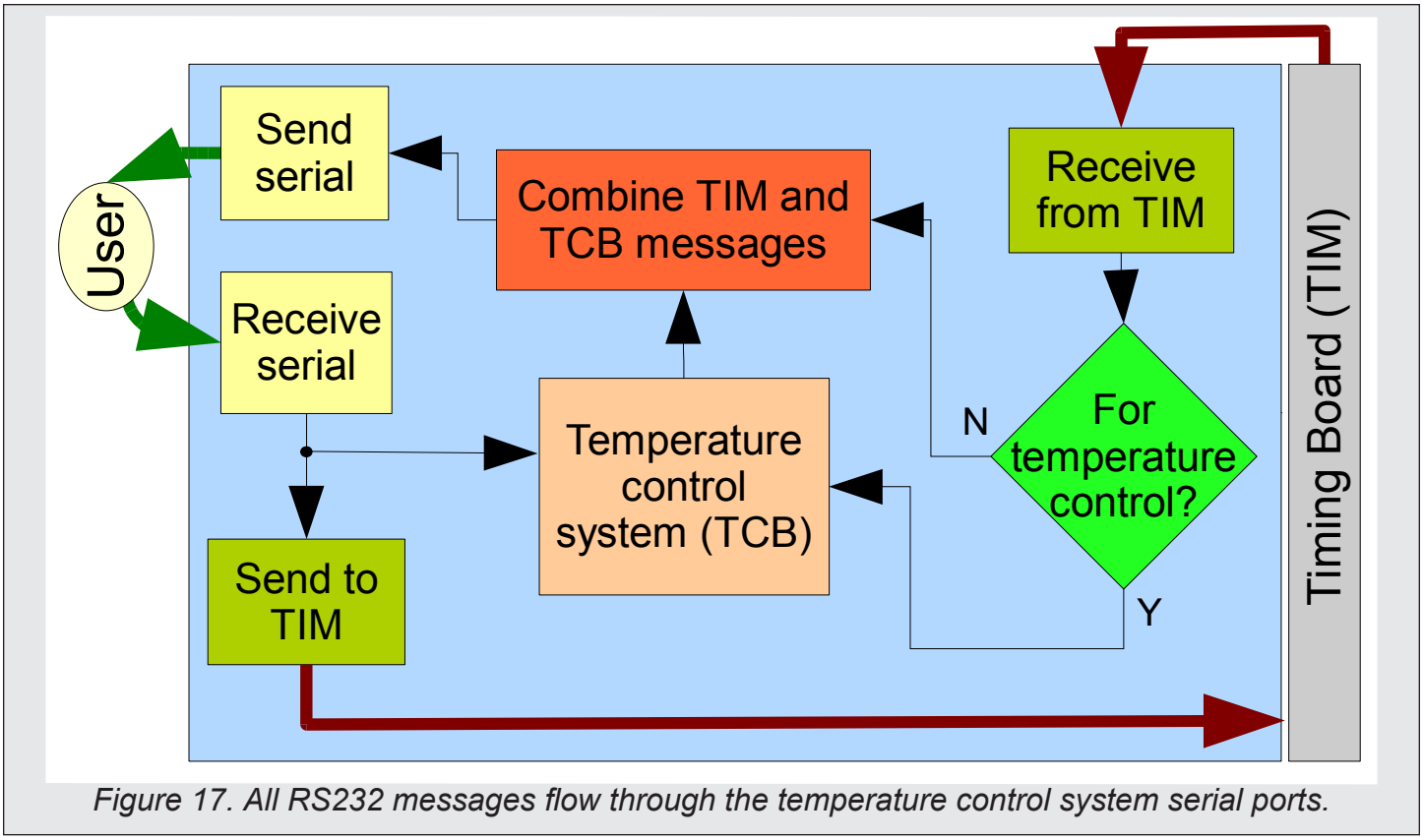


Figure 17. All RS232 messages flow through the temperature control system serial ports.

3.3.2. TIM Version 1

The Timing Board Version 1 is shown in more detail in Figure 18. Version 1 uses the same RS232 serial communications protocol used with the TIM Version 0. All messages to and from the serial port are passed though the temperature control system CPU as outlined in Figure 17.

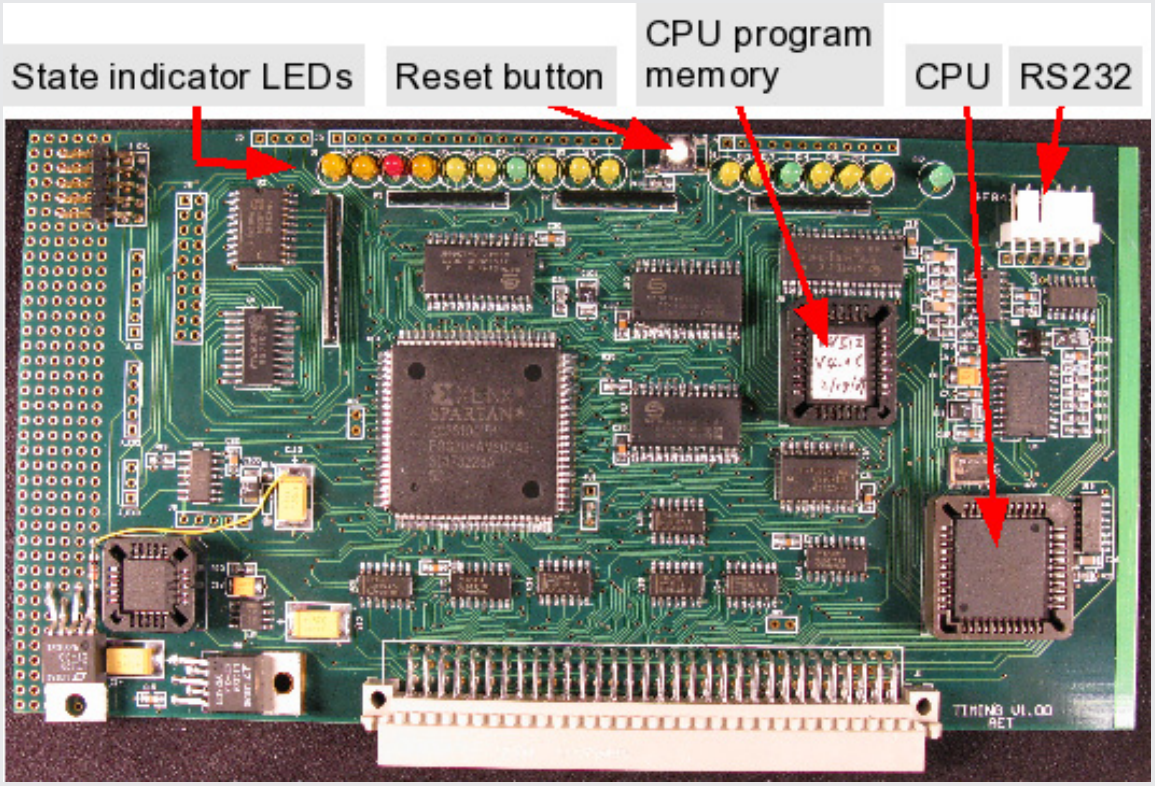


Figure 18. TIM version 1.

Test points for the TIM version 1 are shown in Figure 19. The meaning of the state indicator LEDs is also shown. The test points are discussed in § 12 on page 43

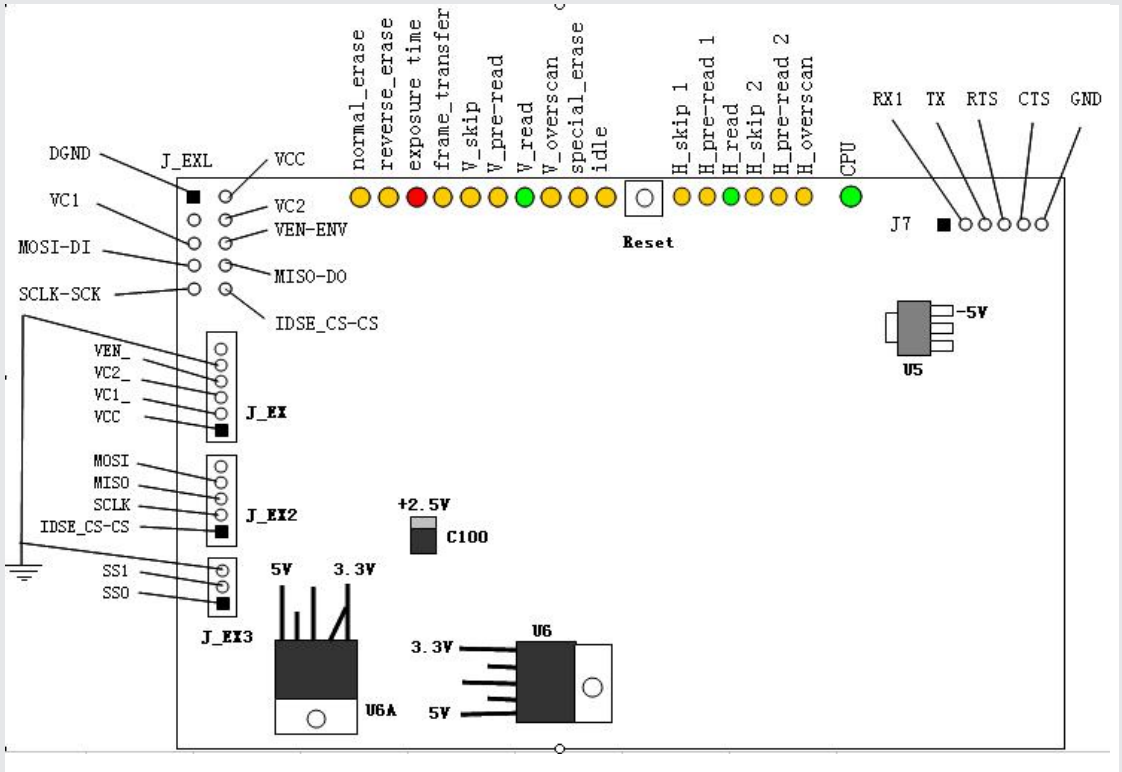


Figure 19. State indicators and various test points for the TIM, version 1.

3.4. CDB

The Clock Driver Board is shown in Figure 20. This board generates all of the signals to the CCD that are intended to change rapidly. For a CCD this typically includes the serial clocks, the parallel clocks, and the transfer gate, summing well and reset gate. The CDB assumes two-level clocks — one high level and one low level. Each clock has two DACs which establish the high and low levels and an analog switch that can select which of the two DAC voltages is applied to the output.

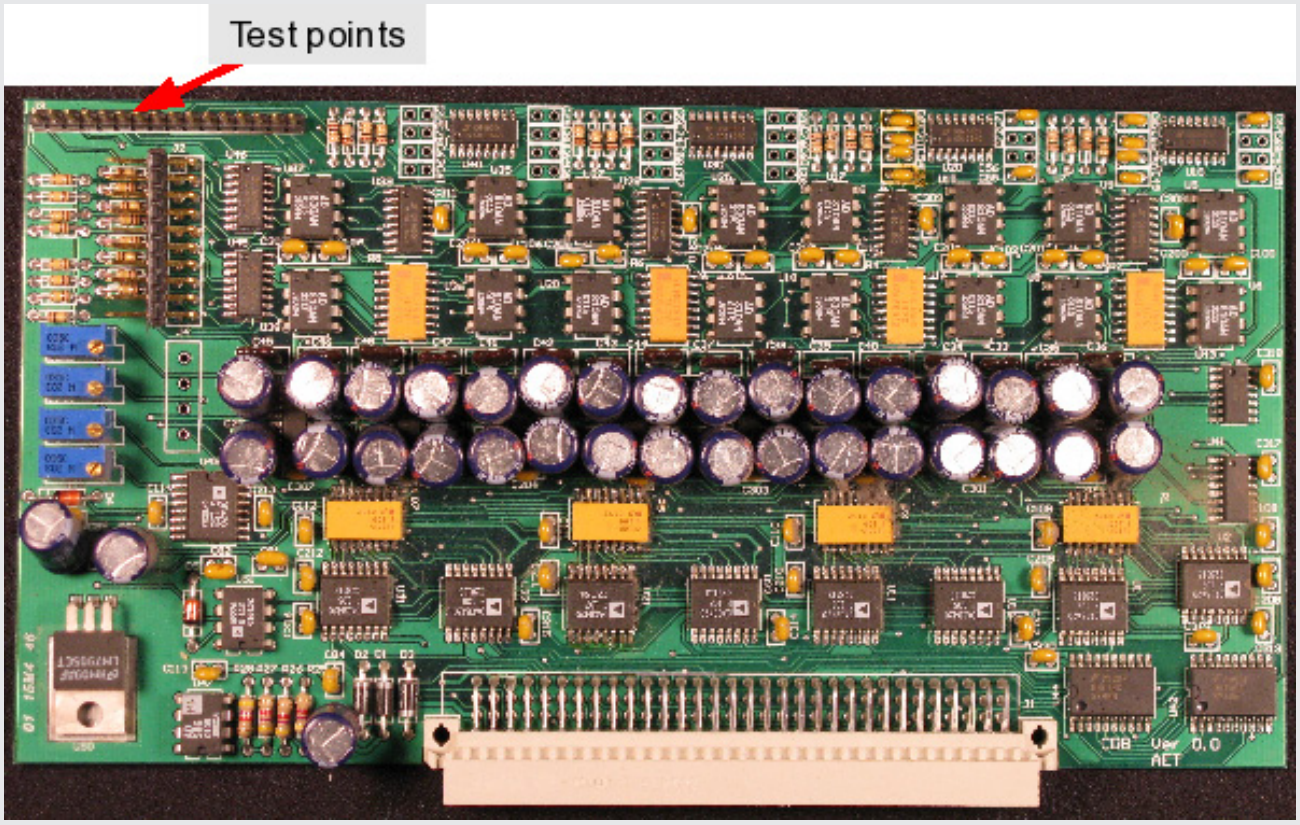


Figure 20. The Clock Driver Board (CDB).

The names for the test points are shown in Figure 21. These same clocks appear on the dual-inline signal connector as shown in the Figure. The cable that plugs into J2 carries the clocks to the dewar interconnect board or, in the case of the Lick guiders directly to the CCD. The names given to the clocks as shown in the Figure are somewhat arbitrary and reflect early usage. But they are not necessarily the names one would assign to these signals for a particular CCD. The characteristics of these clock signals are described in Table 4. The table's **typical use** column describes how these clocks are used in the Lick guiders. But the signal names for clocks used by other CCDs may be different.

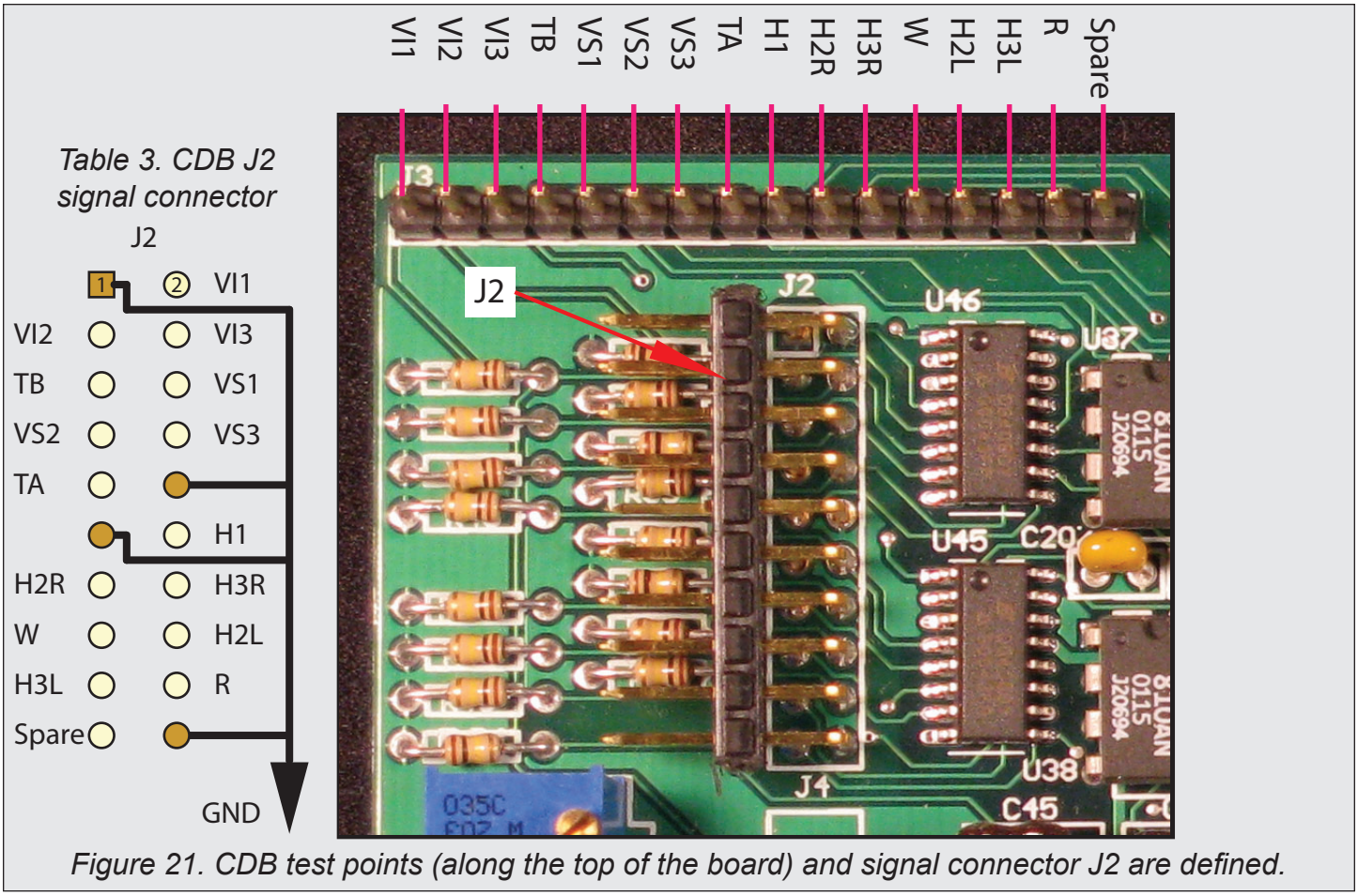


Table 3. CDB J2 signal connector

Figure 21. CDB test points (along the top of the board) and signal connector J2 are defined.

The clocks in Table 4 are color-coded by groups. For the parallel and serial clocks this grouping is significant. Serial and parallel waveforms are defined by look-up tables stored in memory. Within the serial and parallel groups it is possible to electrically assign a particular waveform from the look-up table to one or more J2 output pins. This ability to assign waveforms to output pins results in efficient, compact waveform tables. A full discussion of waveform mapping is given in Section 13.2 on page 54.

UCAM signal name	Nominal Voltage range	Typical use
VI1	-10v — +10v	Parallel clock (Imaging section)
VI2	-10v — +10v	Parallel clock (Imaging section)
VI3	-10v — +10v	Parallel clock (Imaging section)
VS1	-10v — +10v	Parallel clock (Storage section)
VS2	-10v — +10v	Parallel clock (Storage section
VS3	-10v — +10v	Parallel clock (Storage section
TA	-10v — +10v	Transfer gate
TB	-10v — +10v	Transfer gate
H1	-10v — +10v	Serial clock (common phase)
H2R	-10v — +10v	Serial clock
H3R	-10v — +10v	Serial clock
H2L	-10v — +10v	Serial clock
H3L	-10v — +10v	Serial clock
W	-10v — +10v	Summing well
R	-10v — +10v	Reset gate
SPARE	-10v — +10v	Spare

Table 4. The characteristics of the clocks generated by the CDB.

3.5. Signal Processing Boards

The signal processing boards provide video signal processing and nine low-noise bias voltages typically used by CCDs. The video processing schematic is show in Figure 22. The signal from the CCD enters on the left. The preamplifier stage of the processing chain is set to a gain of 5 for the UCO/Lick guiders. For other science CCDs which have a preamplifier board mounted on the dewar the preamp here is set to a gain of 1. In the second stage there are four selectable gain settings. The inverter stage has a 1-bit input which controls whether or not the polarity of the input signal is inverted. This, combined with the Integrator stage performs the Correlated-Double-Sampling (CDS) process. The 1-bit C-Select input selects between two integrator capacitors. The output buffer section includes a 12-bit DAC to provide the desired video signal level out for zero CCD signal in. The output from the signal processing chain is routed by a coaxial cable to the input on an A-to-D converter board (see Section 3.6 on page 29).

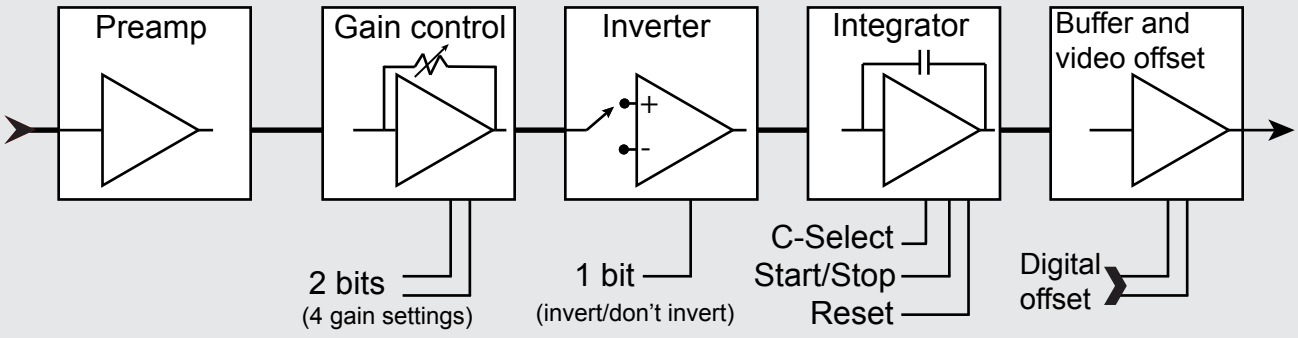


Figure 22. The SPB or DSPB signal processing steps.

The original SPB board has a single video processing chain. The new DSPB has two independent video processing chains.

3.5.1. SPB

The original single channel signal processing board (SPB) is shown in Figure 23. There are two mini-coax connectors near the left edge of the board. One of them is covered by a piece of red tape in Figure 24 and that connector was intended for applications that do not need the onboard preamplifier section of the SPB. But we found we get better noise performance if we always use the preamp section and now we just set the preamp gain to 1X if an external preamp is being used. The second connector on the left is for the video input to the preamp section and is now used whether the signal comes directly from the CCD or from an external preamplifier.

The connector near the upper-right corner of the board is the processed video output from the SPB which goes to an A-to-D converter board. Nine bias voltage test points are also identified in the Figure 23. These test points are labeled in Figure 24. The bias voltages produced by the board are available at the connector pins near the upper left corner of the board. Those pins are shown in detail with labels in Figure 25. As the Figure shows the connector provides +15V and -15V which can be used for an external preamplifier board. There is also an N_{guard} signal (pin 15). This is a special signal originally intended for LBNL high resistivity CCDs and is connected to a digitally-controlled relay which either leaves the N_{guard} open circuit or connects it to analog ground through a 10K Ohm resistor.

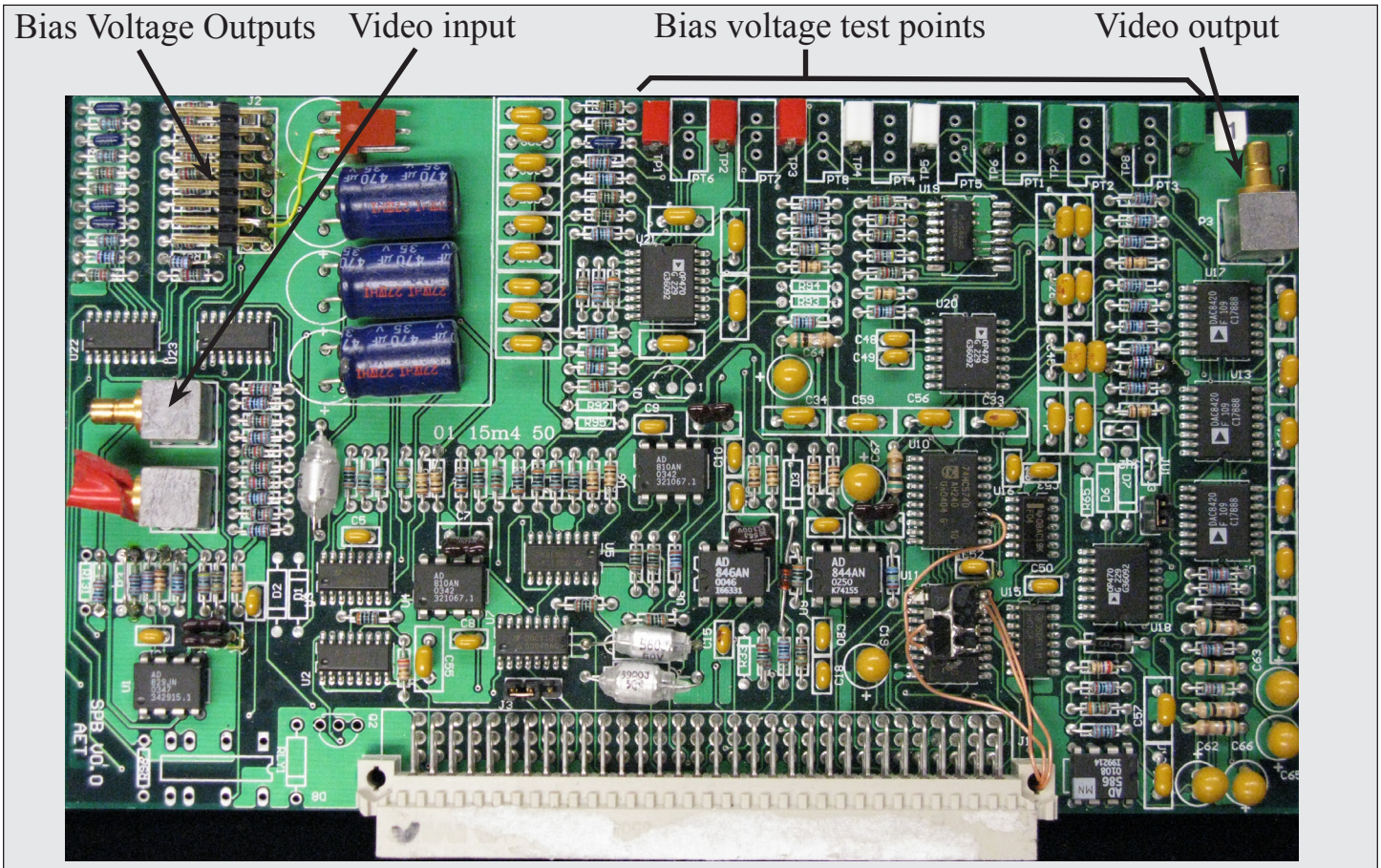


Figure 23. The single channel signal processing board (SPB).

The bias voltage test points labeled in Figure 24 can be examined with an oscilloscope or a volt meter. The voltage ranges are given in Table 5 but the actual voltages depend on what the UCAM controller was commanded to produce. The voltage number shown in the last column of Table 5 is the address of the digital-to-analog converter on the SPB that produces the voltage.

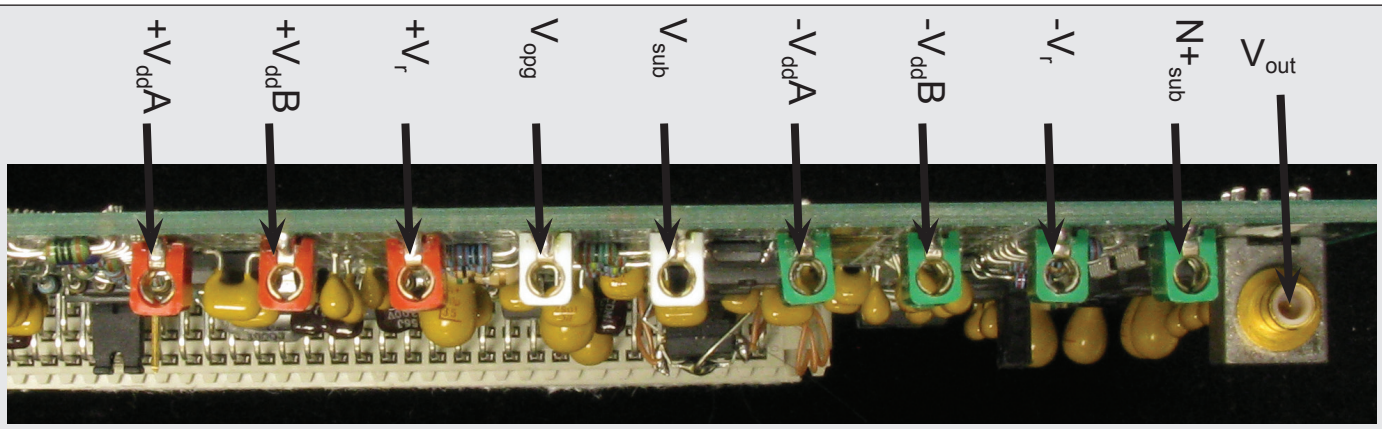


Figure 24. The bias voltage test points at the top of the SPB board.

Voltage name	Typical Usage	Typical Range	Voltage Number
$+V_{dd}A$	Output drain	+6V - +24V	0x80
$+V_{dd}B$	Output drain	+6V - +24V	0x90
$+V_r$	Reset drain	+4V - +18V	0xa0
V_{opg}	Output gate	-6V - +6V	0x60
V_{sub}	Substrate	-5V - +5V	0x70
$-V_{dd}A$	Negative output drain (LBNL CCD)	-9V - -28V	0x00
$-V_{dd}B$	Negative output drain (LBNL CCD)	-9V - -28V	0x10
$-V_r$	Negative reset drain (LBNL CCD)	-6V - -18V	0x20
$N+_{sub}$	Positive substrate (LBNL CCD)		0x50

Table 5. The bias voltages produced on the SPB or DSPB.

The $N+_{sub}$ voltage described in Table 5 and identified at pin 15 in Figure 25 is a special case. This is the substrate voltage for high resistivity CCDs such as those produced by LBNL and the substrate voltage can be very high. The SPB board provides a digital-to-analog converter for this voltage but to generate the final high voltage the DAC output is directed to an auxiliary amplifier which is typically located on the UCAM motherboard. The high-voltage output from this auxiliary circuit is brought back to the SPB where it is distributed to the test point and the bias voltage connector.

Pin #	Bias Voltage
1	+15V Power
2	$+V_{dd}A$
3	$+V_{dd}B$
4	$+V_r$
5	V_{opg}
6	V_{sub}
7	No Conn. (key)
8	Analog Ground
9	-15V Power
10	$-V_{dd}A$
11	$-V_{dd}B$
12	$-V_r$
13	V_{opg}
14	$N+_{sub}$
15	N_{guard}
16	Analog Ground

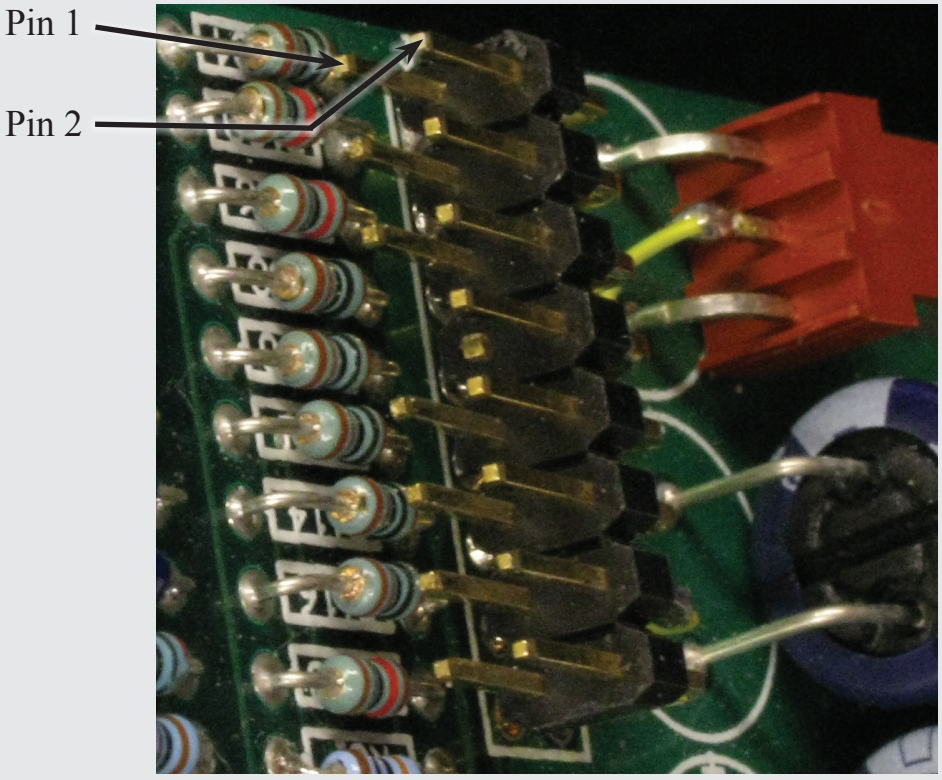


Figure 25. The bias voltage connector on the SPB and DSPB boards. This connector also includes +15V and -15V for powering a preamplifier card.

Note the small, red three-pin molex connector visible in Figure 25. This is the connector for the $N+_{sub}$

high-resistivity CCD voltage. This 3-pin connector is shown in detail in Figure 26.

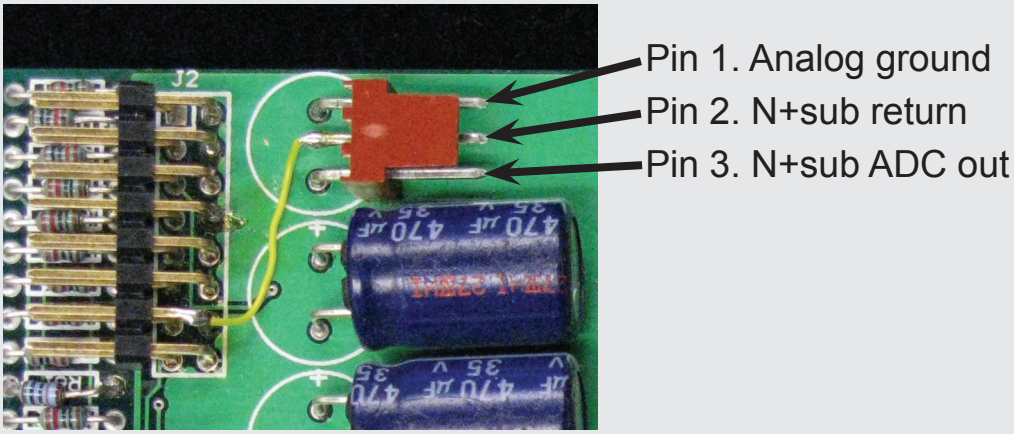


Figure 26. The $N+_{sub}$ connector. The raw ADC output from pin 3 goes to an external circuit which amplifies the voltage and returns the result on pin 2.

It is possible to have at most two SPB boards in a single system. The boards have a board address of either 0 or 1. The board's address is set by the three-pin address selector shown in Figure 27. As shown in the Figure the jumper connects the center pin to the left-most pin and this gives the board address 1. If the jumper connects the center and right-most pin the board has address 0.

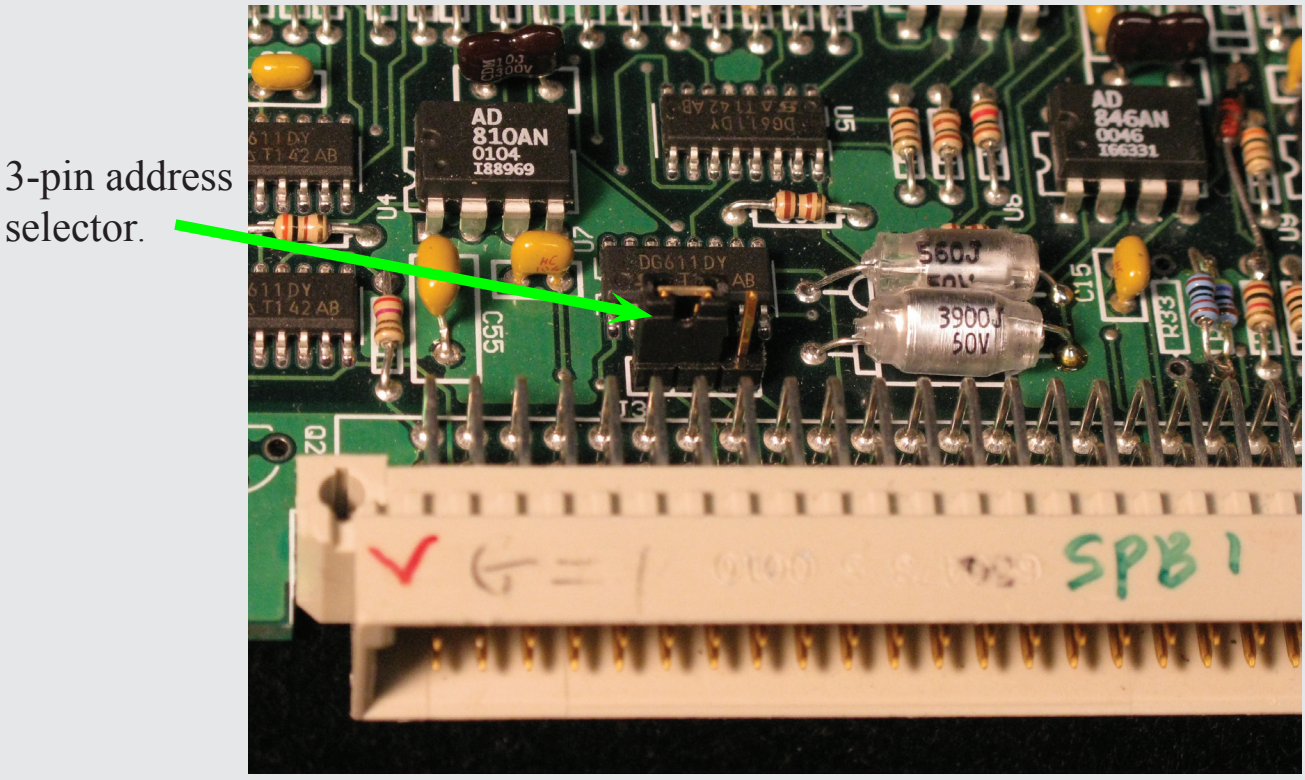


Figure 27. The 3-pin address selector on the SPB. As shown in this figure, with the jumper placed across the middle and left pins the board has address 1.

3.5.2. DSPB

The dual signal processing board is shown in Figure 28. There are two identical video processing channels. The inputs and outputs for the two video channels are labeled A and B in Figure 28.

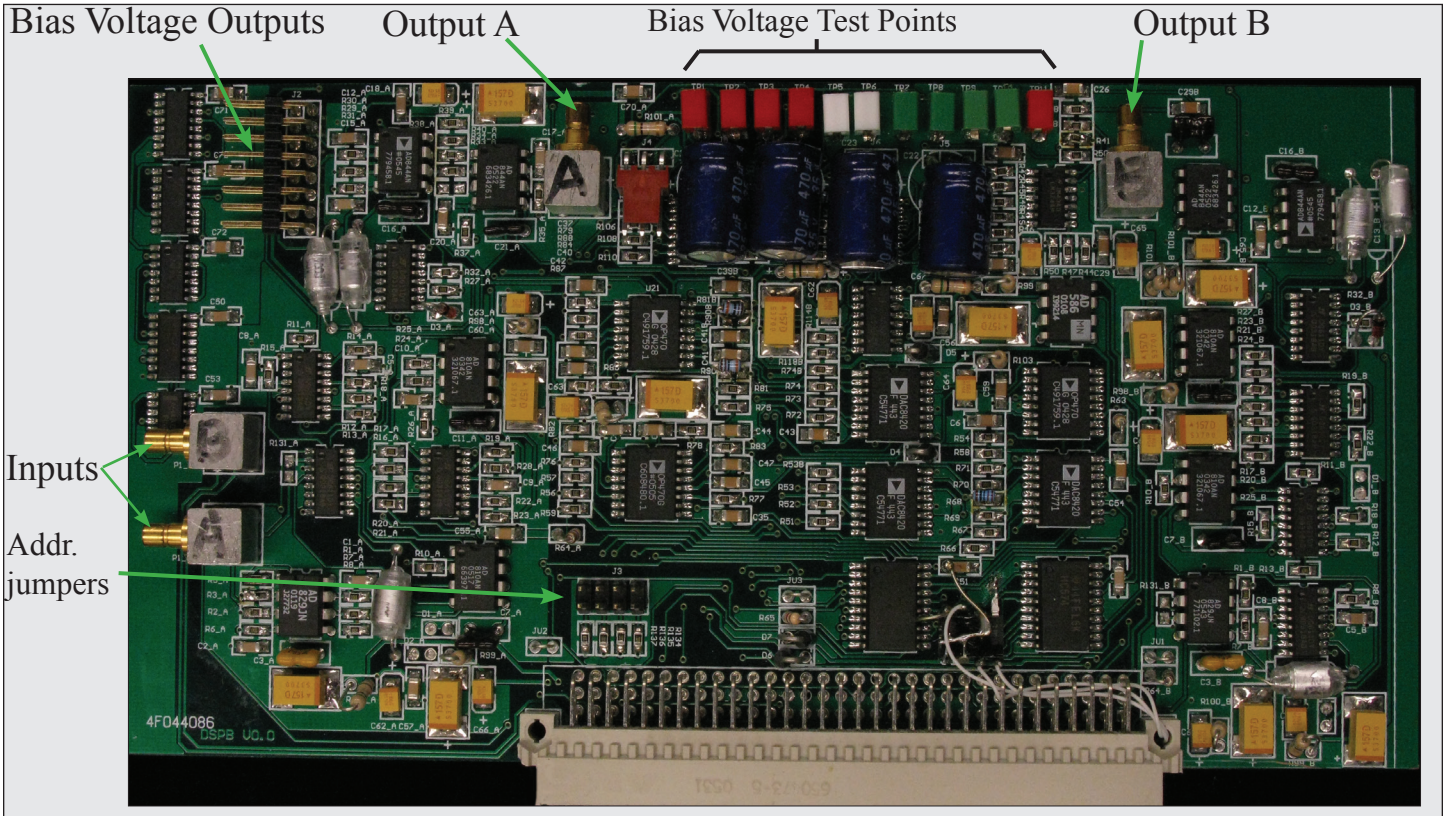


Figure 28. The dual signal processing board.

The DSPB bias voltage test points labeled in Figure 29 can be examined with an oscilloscope or a volt meter. The voltage ranges are given in Table 5 but the actual voltages depend on what the UCAM controller was commanded to produce. The voltage number shown in the last column of Table 5 is the address of the digital-to-analog converter on the DSPB that produces the voltage.

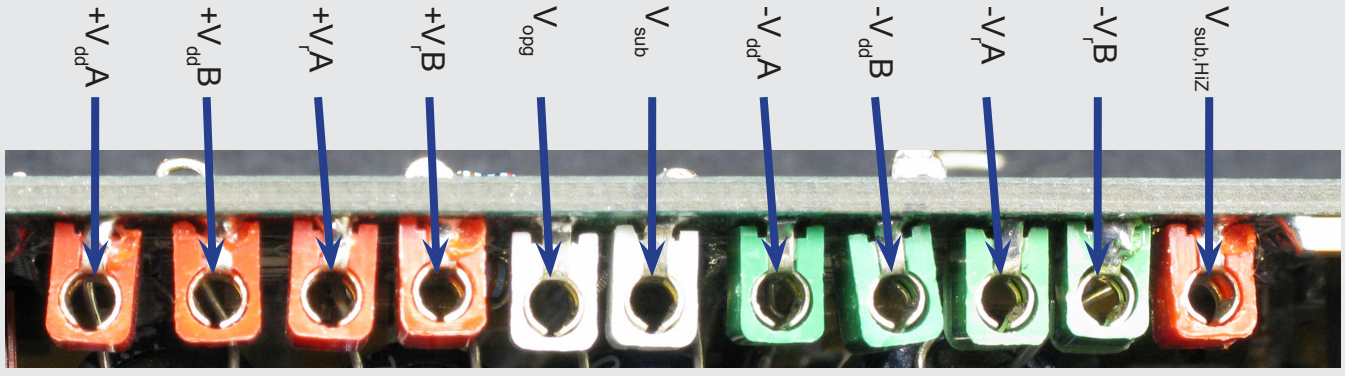


Figure 29. The bias voltage test points at the top of the DSPB board.

The address jumper pins on the DSPB are shown in greater detail in Figure 30.

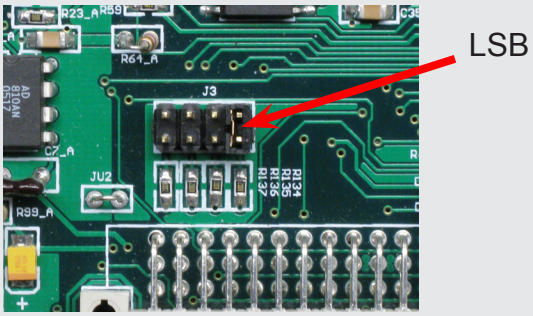


Figure 30. The address pins of the DSPB.

3.6. A-to-D and digital data transmission

The original UCAM analog-to-digital board (referred to as the ADC board) provided two A-to-D converters and a single fiber transmitter for sending the digital video data to the controlling computer. A new board (referred to as the QADC board) was then developed which provides four channels of A-to-D conversion and the same single fiber transmitter. For comparison both boards are show in Figure 31.

The ADC board has no addressing capability which means there can be only one ADC board on the UCAM backplane and such a system cannot support more than two video channels. The QADC board can be assigned an address and therefore more than one QADC board is usable in a single backplane. Even when there are multiple QADC boards all of the digitized video data is routed to just a single fiber transmitter.

Both ADC and QADC use the same fiber transmitter module, the Agilent HFBR 1119ST or equivalent. The fiber connector is a Simplex ST receptacle and can accommodate 62.5/125 µm and 50/125 µm fiber cables. The fiber data are transmitted at a rate of 33 Mbytes per second using the Cypress HOTLink CY7B923 transmitter and CY7B933 receiver (at the computer interface). Three bytes are transmitted per pixel, for a pixel rate of 11 Mpixel per second.

Figure 31. The original ADC board is shown at the top and the newer QADC is shown at the bottom.

3.6.1. ADC board

The ADC board is shown in more detail in Figure 32. There are two mini-coax cable connectors for each input video channel and these two connectors are wired together. The only use of the second connector is as a test point. It can be used for an oscilloscope connection. The corresponding A-to-D converters are also identified in the Figure. The Datel ADS-937 has 16-bit resolution and a 1MHz sampling rate.

Either one or both input channels can be operated. The trigger signal to start the A-to-D conversion is generated by the video processing waveform defined by the user. There is just one start signal, so all channels convert at the same time. At the end of the conversion period the on-board Xilinx FPGA sequences the 16-bit digital data from the A-to-D onto the fiber. With appropriate instructions from the Timing Board CPU the Xilinx FPGA will transmit the data in one of four sequences: A then B, B then A, A only, or B only.

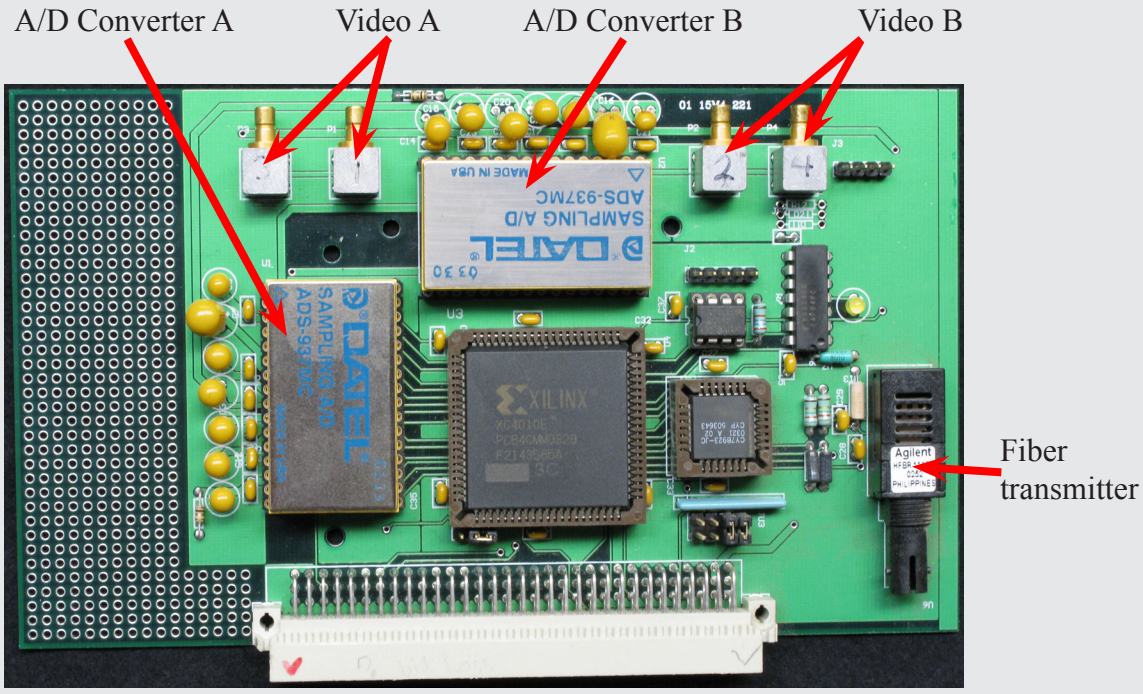


Figure 32. The ADC board. The two video channels are identified.

3.6.2. QADC

The QADC board is shown in more detail in Figure 33. Although the four mini-coax connectors look

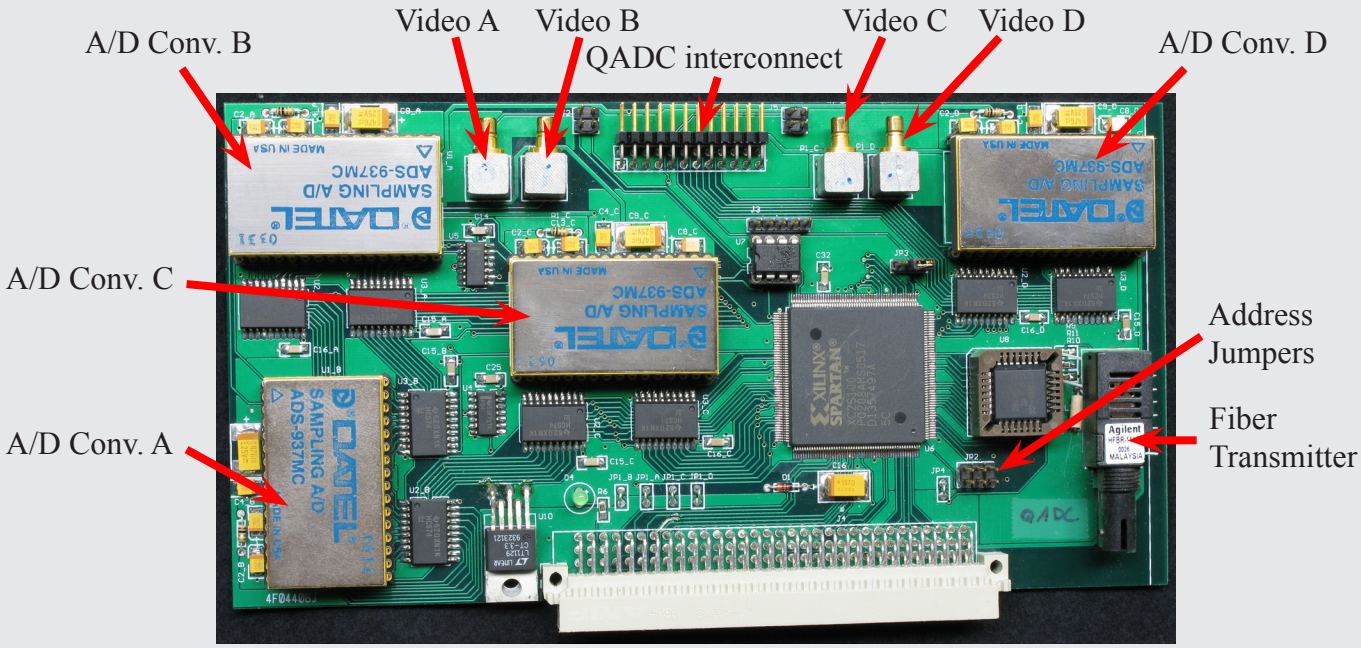


Figure 33. The QADC board. The four video channels and their A/D converters are identified.

like the four connectors on the older ADC board (Figure 32), they are not the same. On the QADC they are the four separate video input channels. Multiple QADC boards can work in a single UCAM controller and to support this capability each board can be assigned a board address. The three address jumper pins are identified in Figure 33. With three bits for an address there can be at most

eight QADC boards in one system. The board shown has all jumpers removed from the pins and this is address 0. The most significant bit is to the right in the Figure.

When more than one QADC is used in a controller the board with address 0 is designated as the master QADC. The other boards are slave QADC boards. They do not have a fiber transmitter and their Xilinx FPGA is programmed to act as a slave. When there is just one QADC in a controller that is a master but there are no slaves.

The Xilinx FPGA of the master is used to sequence the digital data from the ADCs onto the fiber transmitter. Instructions from the Timing board define which ADCs are transmitted over the fiber and they define the order in which they are transmitted. When there are two or more QADC boards in a system a ribbon cable is plugged into the QADC interconnect (see Figure 33 and Figure 35) to form a local bus between the boards. The master Xilinx reads data from the other boards over the interconnect cable. The optical fiber interface operates at 11 Mpixels per second, or 0.091 microseconds per pixel. A four channel UCAM controller would transmit all four pixels in about 0.4 microseconds.

The pin definitions for the interconnect board are shown in Figure 34 and Table 6. The interconnect is very simple with 16 data bits and 5 QADC board select bits. The master Xilinx places a board number on the select pins, waits a short setup time, and then reads the 16-bit data word placed on the bus by the addressed board. (There is no error checking.)

Table 6. The QADC interconnect pins.

Pin	Function	Pin	Function
1	GND	2	ADCD0
3	ADCD1	4	ADCD2
5	ADCD3	6	ADCD4
7	ADCD5	8	ADCD6
9	ADCD7	10	ADCD8
11	ADCD9	12	ADCD10
13	ADCD11	14	ADCD12
15	ADCD13	16	ADCD14
17	ADCD15	18	SELI00
19	SELI01	20	SELI02
21	SELI03	22	SELI04
23	N.C.	24	GND

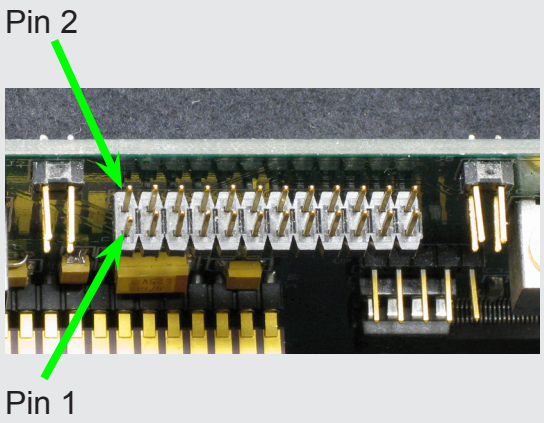


Figure 34. The QADC interconnect connector with pin definitions.

Each QADC has a set of four video test points as shown in Figure 35. These test points are wired to the video input mini-coax connectors. In the Lick UCAM systems these test points may be brought out to coax connectors on the side of the UCAM controller housing.

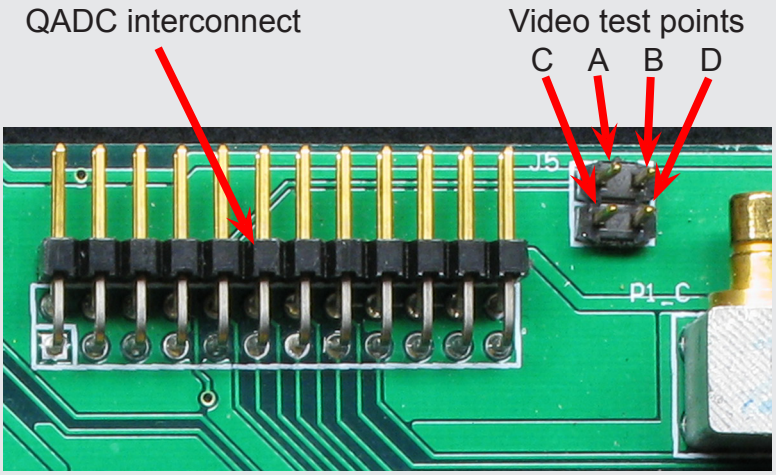


Figure 35. The video test points on the QADC.

There is a similar set of four test points to the left of the QADC interconnect. Those test points are visible in Figure 33 and Figure 34. These test points are digital test points wired to four output bits of the Xilinx FPGA. Since the Xilinx is programmable these test points do not have a fixed function. Instead they can be used to probe any internal points in the Xilinx by appropriate Xilinx programming.

3.6.3. Replacement A-to-D Converter

The Datel ADS-937 analog to digital converter used on the ADC and QADC boards is a high quality A-to-D but it is an old design that is expensive and that dissipates significant power in the form of heat. As a plug-compatible replacement we have designed an alternate A-to-D module which is shown in Figure 36. This module plugs into the same socket occupied by the ADS-937. It uses the Analog Devices AD7677 ADC. This ADC uses much less power than the old Datel part so it reduces the current demands on the power supplies and it produces much less heat. Performance for the AD7677 is similar to the ADS-937.

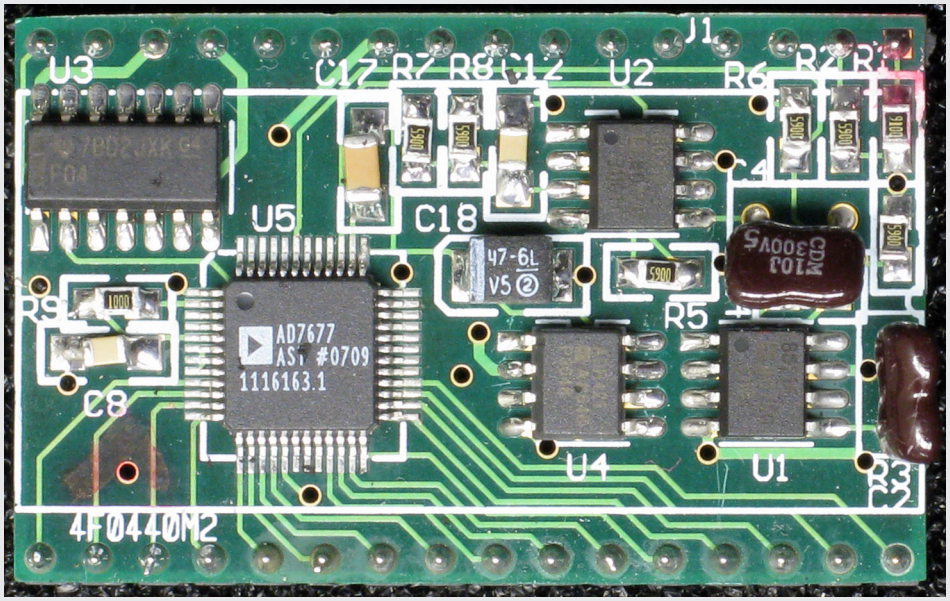


Figure 36. The A-to-D module using the Analog Devices AD7677 replaces the older Datel ADS-937.

4. Power Supply Components

The power supply pictured in Figure 5 (page 7) and Figure 6 is shown with the top removed in Figure 37.

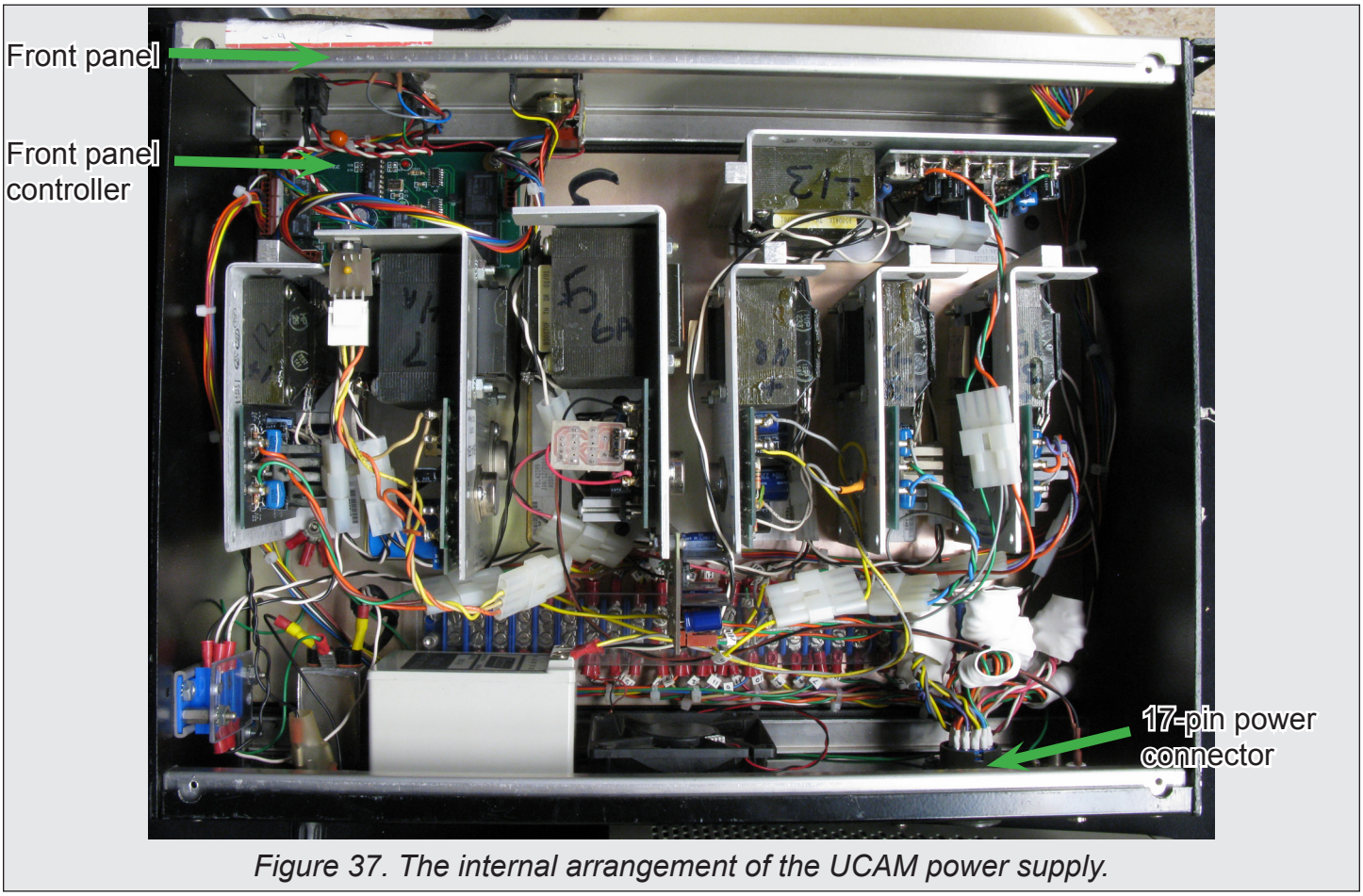


Figure 37. The internal arrangement of the UCAM power supply.

5. Dewar Interface Components

6. Computer Interface Components

6.1. PCI Interface

Figure 8 on page 10 shows all of the detail necessary to use the PCI interface. There is really just one fiber connector on the card which is used with the UCAM controller.

6.2. USB Interface

The connectors of the USB fiber interface are shown in Figure 38. In the usual installation only serial port 0 is used. The more recently built USB interfaces do not include the second serial port or the second fiber port. The small power supply for the USB interface is also shown in the Figure. We use a

6-volt DC supply to keep power dissipation low.

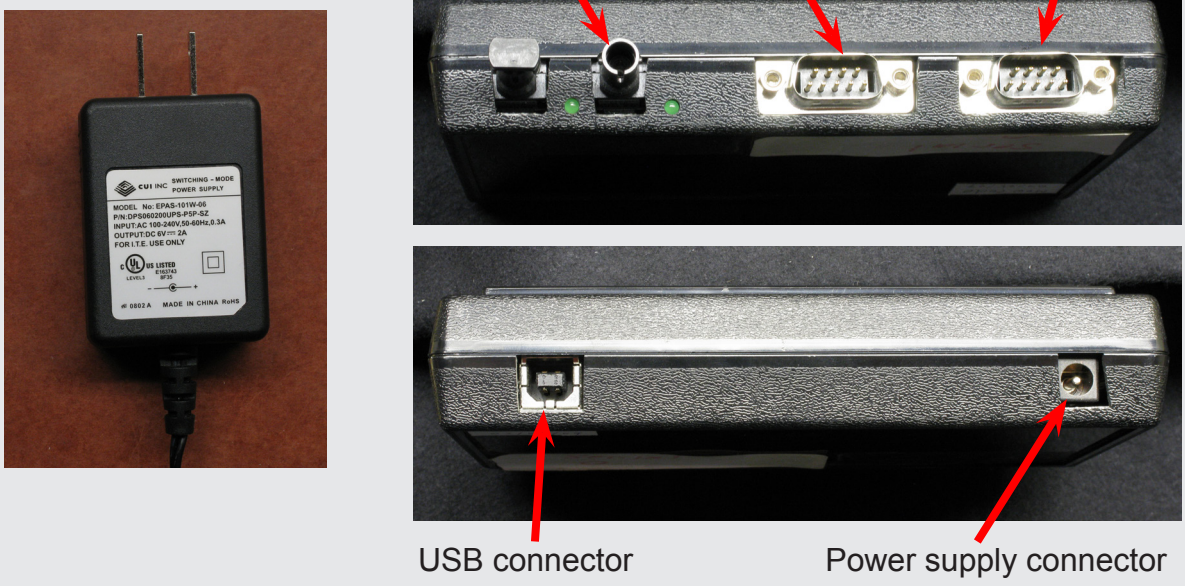


Figure 38. The details of the USB fiber interface connectors.

7. Temperature Measurement and Control

7.1. Introduction

The UCAM controller can measure two temperatures, an external temperature and an internal temperature. The external temperature is typically the CCD temperature and the internal temperature is the temperature inside the UCAM enclosure. The temperature measurement relies on the observation that the voltage across a forward-biased diode is linearly related to the temperature of the diode. One diode is mounted inside the UCAM enclosure for the internal temperature. Another diode is mounted somewhere in close thermal contact with the CCD. Each diode must be calibrated. Calibration of a diode involves measuring the voltage across the diode at two temperatures. The linear relationship derived from these two temperatures can then be used to infer a temperature for any other measured voltage.

The temperature is displayed on the front panel of the UCAM power supply as illustrated in Figure 39. This display uses a simple digital volt meter. To achieve an accurate temperature display this meter must be calibrated.

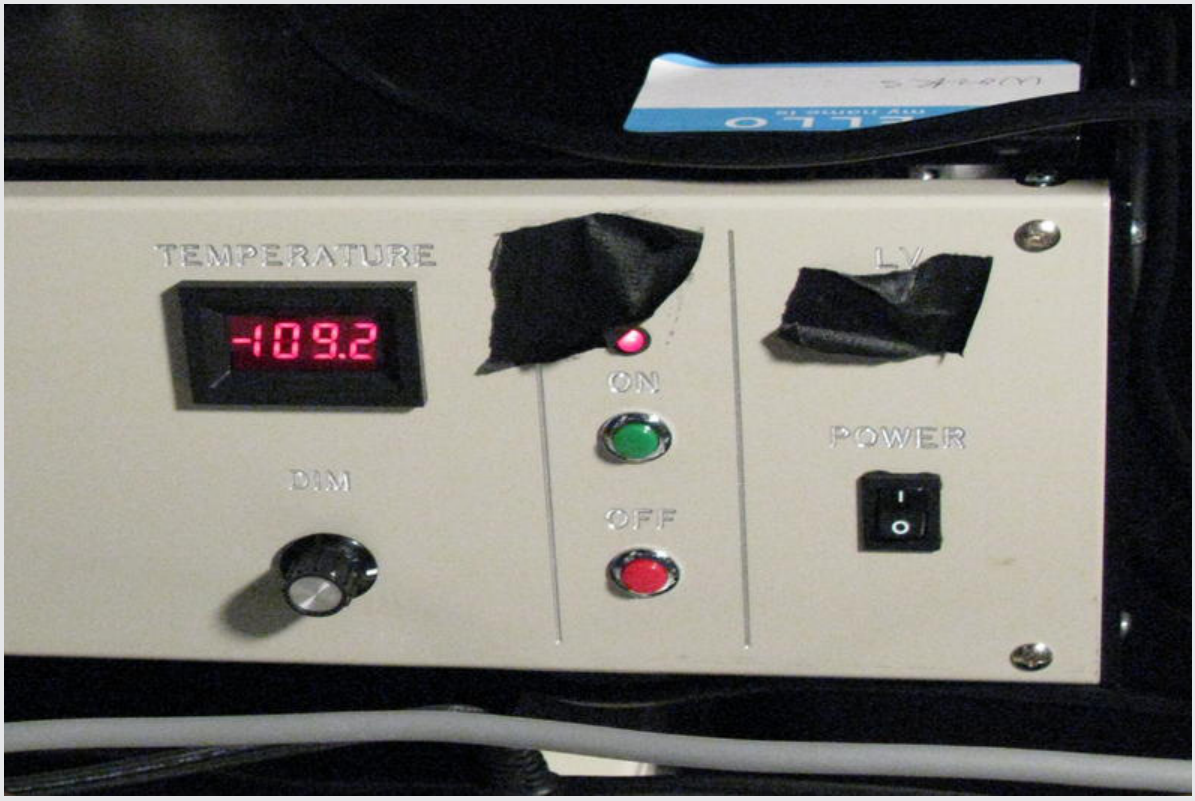


Figure 39. Power supply front panel meter showing CCD temperature.

7.2. Temperature Display Calibration

To do all of the calibrations a simple terminal emulation program is needed to communicate with the UCAM serial port. In the CCD lab we use either a laptop connected directly to the serial port of the UCAM controller or the **uterm** terminal emulation program communicating through the workstation serial port used by the UCAM gui software. The gui software must not be running at the same time. To calibrate the temperature display start the terminal emulation program. The following shows the typical dialog to carry out the calibration.

```
&CAM
T=(SDDD.D)+157.1
+157.1 OK
T=(SDDD.D)-157.9
-157.9 OK
```

Your typing is colored blue and the controller's response is colored brown. If the terminal emulation program does not echo your characters locally then you will not see what you are typing because the controller does not echo your characters either. The calibration process is started by typing the command &CAM. Read the number from the display and enter it exactly as show with a sign (+ or -), three digits, a decimal point, and another digit. If you are using the uterm program you need to type the Enter key too. Then a second number is shown on the display and you enter that number exactly as shown (plus Enter if using uterm). That's all there is to the calibration.

7.3. Diode Calibration

It is possible to calibrate the temperature measurement circuitry using the actual diodes that are going to be employed with the CCD and controller (method 1) or to calibrate using different diodes with characteristics identical to the ones that are used with the CCD and controller (method 2). In the UCO/Lick CCD lab we have a collection of identical diodes so we often find it more convenient to use method 2. But this might not always be possible if, for instance you have a unique diode mounted on the CCD.

The diodes are connected to the controller at the location shown in Figure 11 on page 14.

8. Cabling

8.1. Local voltage regulators

8.2. External connectors and cables

8.2.1. Power Supply Cable

The 17-pin power connector (Amphenol 97-3100A layout 20-29 or equivalent) on the back of the power supply (Figure 6 on page 8) is cabled to the UCAM controller with AWM style 2464 double-shielded, 12-gauge wire cable. The pin definitions for the connector are given in Table 7.

Pin #	Voltage Name	Ground Reference*	Pin #	Voltage Name	Ground Reference*
A	+48V	AGND	K	+5VCC	DGND
B	-30V	AGND	L	+14VC	AGND
C	-14VC	AGND	M	+30V	AGND
D	+7VB	GNDB	N	AGND	
E	-6VA	AGND	P	-15VA	AGND
F	+15VA	AGND	R	GNDB	
G	T (+) (temp. readout)	GNDB	S	DGND	
H	+12VB	GNDB	T	+6VA	AGND
J	-12VB	GNDB			
*AGND=analog ground DGND=digital ground, GNDB=Independent ground for the TCB system.					

Table 7. Definitions for the 17-pin power cable.

The cable has more than 17 wires and one of the extra wires is used as a $+5V_{CC}$ sense feedback to the 5V supply inside the power supply chassis. This feedback signal is brought into the BNC connector labeled in Figure 6 and shown connected to the cable in Figure 40. Also note that the power cable shield is connected to the power supply chassis ground with the banana plug.

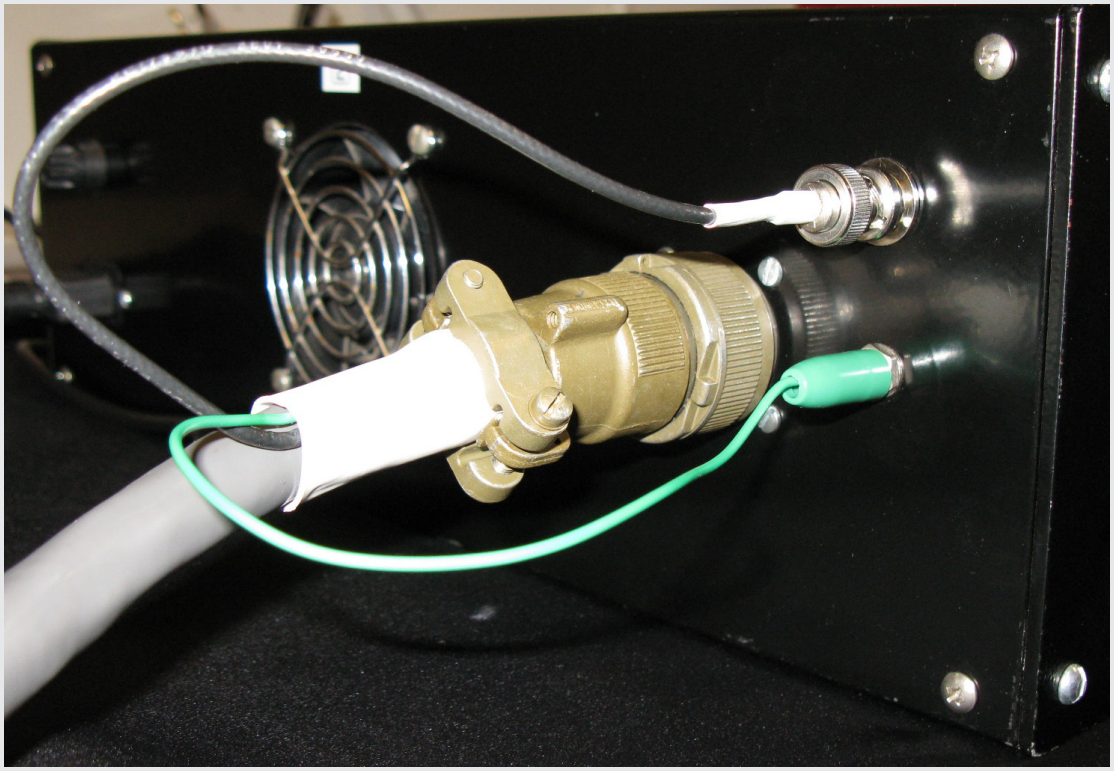


Figure 40. The +5VCC sense feedback is connected to the BNC connector and the power supply shield in connected to the power supply chassis ground by the banana plug.

8.2.2. DB37 Cable

The UCAM controller is connected to the preamp box with a 37-pin cable and a 25-pin cable. The 37-pin cable uses a DB-37 style connector and the pin definitions for the connector are given in Table 8. The 25-pin cable is described in the next section. All of the entries in Table 8 with a green background are analog signals or grounds. All of the entries with a blue background are digital signals.

Signal Name	Pin#	Typical Function	Notes
VI1_in	J1-1	Parallel clock	twisted with J1-20
GND	J1-20 to J1-34		J1-20 through J1-34 are analog ground pins
VI2_in	J1-2	Parallel clock	twisted with J1-21
VI3_in	J1-3	Parallel clock	twisted with J1-22
TB_in	J1-4	Tranfer gate B	twisted with J1-23
VS1_in	J1-5	Parallel clock	twisted with J1-24
VS2_in	J1-6	Parallel clock	twisted with J1-25
VS3_in	J1-7	Parallel clock	twisted with J1-26
TA_in	J1-8	Transfer gate A	twisted with J1-27
H1_in	J1-9	Common serial clock	twisted with J1-28
H2R_in	J1-10	Serial clock	twisted with J1-29
H3R_in	J1-11	Serial clock	twisted with J1-30
w_in	J1-12	Summing well	twisted with J1-31
H2L_in	J1-13	Serial clock	twisted with J1-32
H3L_in	J1-14	Serial clock	twisted with J1-33
R_in	J1-15	Reset gate	twisted with J1-34
VC1_	J1-16		twisted with J1-35
VC2_	J1-17		twisted with J1-36
DGND	J1-35		This is digital ground
DGND	J1-36		This is digital ground
$\overline{\text{ENV}}$	J1-18		
V_{cc}	J1-19		
V_{cc}	J1-37		

Table 8. Pin definitions for the DB37 cable from the UCAM controller to the preamp box. Green denotes analog signals and blue denotes digital signals.

8.2.3. DB25 Cable

The UCAM controller is connected to the preamp box with a 37-pin cable and a 25-pin cable. The 25-pin cable uses a DB-25 style connector and the pin definitions for the connector are given in Table 9. The 37-pin cable is described in the previous section.

Signal Name in oldPREAMP	Signal Name in PRE-INT	Pin#	Notes
+15v	+15V	J2-1	Preamp power
+VDDA_in	+VddA1	J2-14	
+VRA_in	+VRA1	J2-2	
VOPGA_in	VOPG0	J2-15	
VSUB_in	VSUB0	J2-3	
GND	GND	J2-16	
-15v	-15V	J2-4	
-VddA_in	-VddA0	J2-17	
-VRA_in	-VRA0	J2-5	
n+Vsub	N+SUB1	J2-18	
+VDDB_in	+VddB1	J2-6	
+VRB_in	+VddA0	J2-19	
VOPGB_in	VOPG1	J2-7	
GND	GND	J2-20	
-VddB_in	-VddA1	J2-8	
VRB_in	+VddB0	J2-21	
		J2-9	No connection
CS_	CS_	J2-22	Serial eprom chip select
SCK	SCK	J2-10	Serial eprom clock
DO	DO	J2-23	Serial eprom data
DI	D1	J2-11	Serial eprom data
HEAT+	HEAT+	J2-24	CCD temperature control
HEAT-	HEAT_	J2-12	CCD temperature control
TEMP+	TEMP+	J2-25	CCD temperature sensor input
TEMP-	TEMP_	J2-13	CCD temperature sensor input

Table 9. Pin definitions for the DB25 cable from the UCAM controller to the preamp box.

8.3. Internal connectors and cables

8.3.1. DB37 to CDB Molex

The external DB37 cable described in Table 8 connects internally to the Clock Driver Board (CDB). The internal cable is described in Table 10.

Signal Name	DB37 Pin#	Pin # of CDB board (voltage code)
VI1_in	J1-1	CDB-J2-2 (CA00)
GND	J1-20	CDB-J2-1
VI2_in	J1-2	CDB-J2-3 (CA10)
GND	J1-21	
VI3_in	J1-3	CDB-J2-4 (CA20)
GND	J1-22	
TB_in	J1-4	CDB-J2-5 (CA30)
GND	J1-23	
VS1_in	J1-5	CDB-J2-6 (CA40)
GND	J1-24	
VS2_in	J1-6	CDB-J2-7 (CA50)
GND	J1-25	
VS3_in	J1-7	CDB-J2-8 (CA60)
GND	J1-26	
TA_in	J1-8	CDB-J2-9 (CA70)
GND	J1-27	
H1_in	J1-9	CDB-J2-12 (CA80)
GND	J1-28	
H2R_in	J1-10	CDB-J2-13 (CA90)
GND	J1-29	
H3R_in	J1-11	CDB-J2-14 (CAA0)
GND	J1-30	
w_in	J1-12	CDB-J2-15 (CAB0)
GND	J1-31	
H2L_in	J1-13	CDB-J2-16 (CAC0)
GND	J1-32	
H3L_in	J1-14	CDB-J2-17 (CAD0)
GND	J1-33	
R_in	J1-15	CDB-J2-18 (CAE0)
GND	J1-34	CDB-J2-20
VC1_	J1-16	JAUX-5,TIMING-J-EX-2 *
DGND	J1-35	JAUX-1,TIMING-J-EX-5
VC2_	J1-17	JAUX-4,TIMING-J-EX-3
DGND	J1-36	
ENV_	J1-18	JAUX-6,TIMING-J-EX-4
VCC	J1-19	JAUX-2,TIMING-J-EX-1
VCC	J1-37	

Table 10. Internal cabling from the DB37 connector to the CDB Molex connector.

8.4. Backplane power

8.4.1. Power Supply Connectors

Connectors J1 and J4 on the motherboard extension are power supply connectors.

J4

1-2	+5 V_{CC}
3-4	GNDD
5-6	+7V
7-8	GNDB

Table 11. J4 Power connector

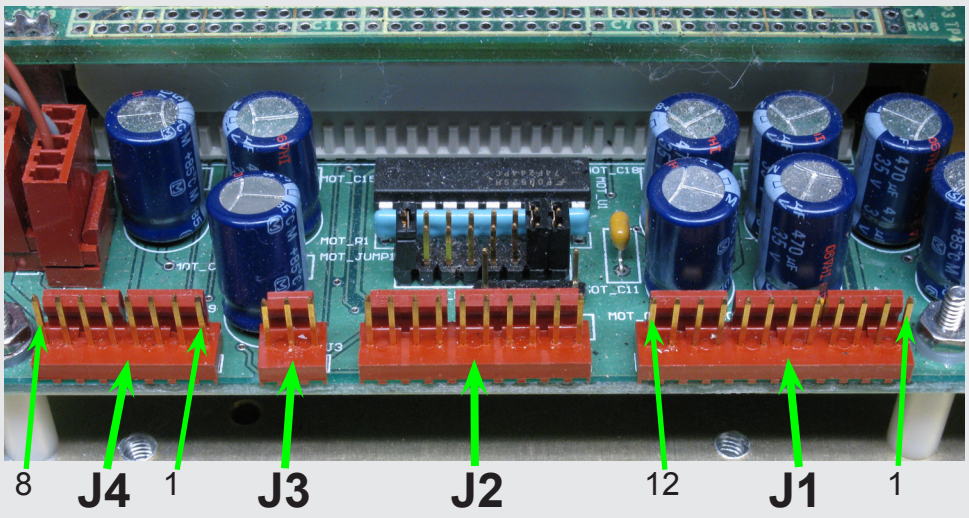


Figure 41. Interconnect board connectors

J1

1	GND
2	+48V
3	-28V
4	+14V
5	+5V
6	-5V
7	-14V
8	-28V
9	+12V
10	-12V
11	NC
12	GND

Table 12. J1 Power connector

9. Controller Software

The UCAM 8051 is programmed entirely in assembly language.

10. Voltages

10.1. Voltage Calibrations

10.2. Voltage files

11. CCD-Specific Serial Eproms

11.1. Introduction

11.2. Cables

11.3. Data formats

11.4. Saving and reading parameters

12. Diagnostics

12.1. Backplane Voltage Test Points

12.2. Clock Driver Board

12.3. Signal Processing Board

13. Waveforms

Typical CCDs have a set of serial clock waveforms and a set of parallel clock waveforms. The Xilinx

FPGA design files for the UCAM controller assume there are six serial clocks and it uses the labels H1, H2R, H3R, H2L, H3L, and SPARE for these serial clocks. One might assume that L and R stand for Left and Right and 1, 2, and 3 refer to serial clock phases, and that would be correct for some configurations. But the controller is really far more flexible and these unfortunate choices for labels may lead to confusion unless the user is careful.

A similar situation exists for the parallel clocks, which are labeled in the FPGA design files as VI1, VI2, VI3, VS1, VS2, and VS3. Here one might assume that I stands for Imaging area and S stands for Storage area (in a frame store capable CCD) and 1, 2, and 3 refer to parallel clock phases. Again this might be correct for some configurations but it is not necessarily true.

These serial and parallel clock labels are used in Table 3 and Figure 21 on page 23 which shows the Clock Driver Board (CDB) and its output connector. They do not necessarily match the labels used by CCD manufacturers.

In the UCAM controller clock waveforms are strictly two-level clocks. An analog switch is used to select between two voltage levels. Therefore a single digital bit can be used to switch between one voltage level and the other.

The bits that define the various waveforms are manipulated within the Xilinx FPGA as three 8-bit registers. One register controls the serial clocks, one controls the video processing waveform, and one controls the parallel clocks. The Xilinx sequentially copies 8-bit byte values from a table of values in memory into the 8-bit registers to create the waveforms.

The bits for the serial (Table 13), video processing (Table 14), and parallel clocking (Table 15) are described below. The serial waveform byte includes control bits for the reset pulse and the summing well. There are three unused bits in the serial waveform byte.

Clock name	Byte(hex)	Bit(binary)
h1	1	00000001
h2	2	00000010
h3	4	00000100
reset	8	00001000
well	10	00010000
no_use1	20	00100000
no_use2	40	01000000
no_use3	80	10000000

Table 13. Definitions of the serial clock waveform bits.

Because video processing and serial clocking are usually overlapping to some extent, a new video processing waveform byte is always applied by the Xilinx at the same time a new serial clocking waveform byte is applied. Therefore for every serial clocking waveform byte there must be a corresponding video processing waveform byte to define the state of the video processing hardware.

Clock name	Byte(hex)	Bit(binary)
clamp	1	00000001
sample	2	00000010
pol	4	00000100
pol_	8	00001000
dcrs	10	00010000
stadc	20	00100000
stsam	40	01000000
onep	80	10000000

Table 14. Definitions of the video processing waveform bits.

Clock name	Byte(hex)	Bit(binary)
v1	1	00000001
v2	2	00000010
v3	4	00000100
vs1	8	00001000
vs2l	10	00010000
vs3	20	00100000
vt	40	01000000
oner	80	10000000

Table 15. Definitions of the parallel clock waveform bits.

The careful reader may note that Table 13 shows only three serial clocks, H1, H2, and H3 instead of the six serial clocks indicated by the CDB output pin definitions in Table 3 on page 23. The three internal serial clocks are turned into the six output serial clocks by the signal-routing schematic circuit shown in Figure 42. Each output pin has its own signal-routing circuit.

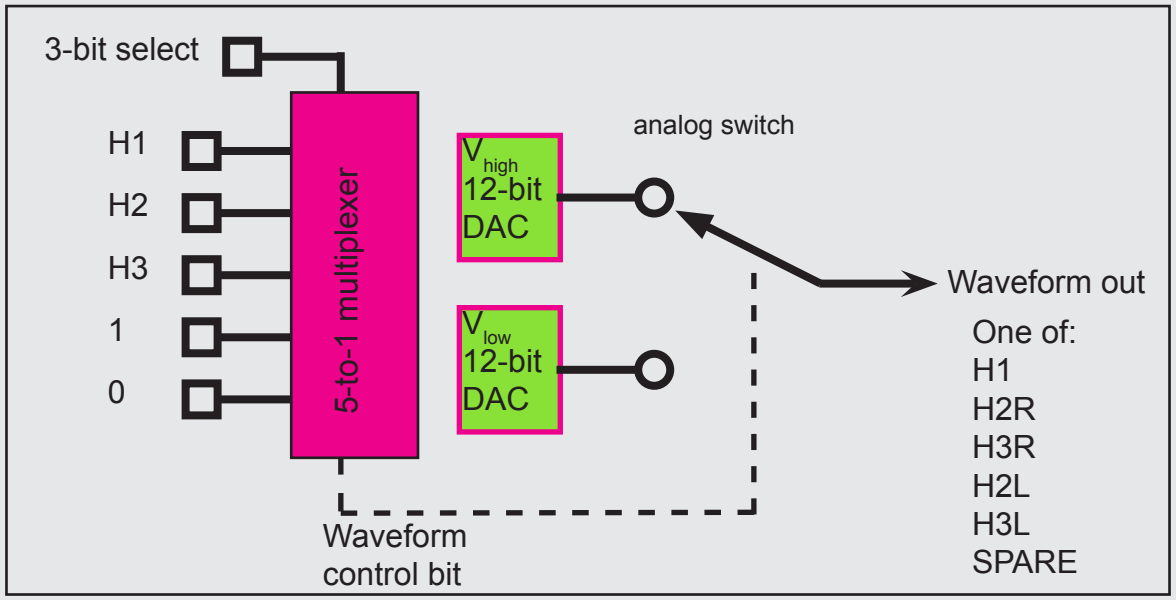


Figure 42. Each serial output pin has a circuit similar to this one which selects one of the waveform table bits as the control for that output pin.

With the circuit in Figure 42 any of the internal serial clocks can be routed to any of the output pins, or any of the output pins can be held in the high or low voltage state. A 3-bit selection value control which of the five inputs of the multiplexer is routed to the output. The 3-bit selection values are shown in Table 16.

selection value	Input bit selected
1	H1
2	H2
3	H3
4	1
5	0

Table 16. Selection values for the serial clocks.

This logic makes for very compact internal waveforms and it works for the vast majority of CCDs. It does assume that there are just three independent serial clock patterns that are routed to the external pins in various combinations. For CCDs (or other types of detectors) with more complex clocking this may be seen as a fundamental limitation of the UCAM design.

There are similar multiplexer circuits for each of the parallel clock pins shown in Table 3. In the case of the parallel clocks waveform bits detailed in Table 15 there are two sets of three waveform bits: V1, V2, and V3 in one group and VS1, VS2, and VS3 in the other. The multiplexer circuits are shown in Figure 43 and Figure 44.

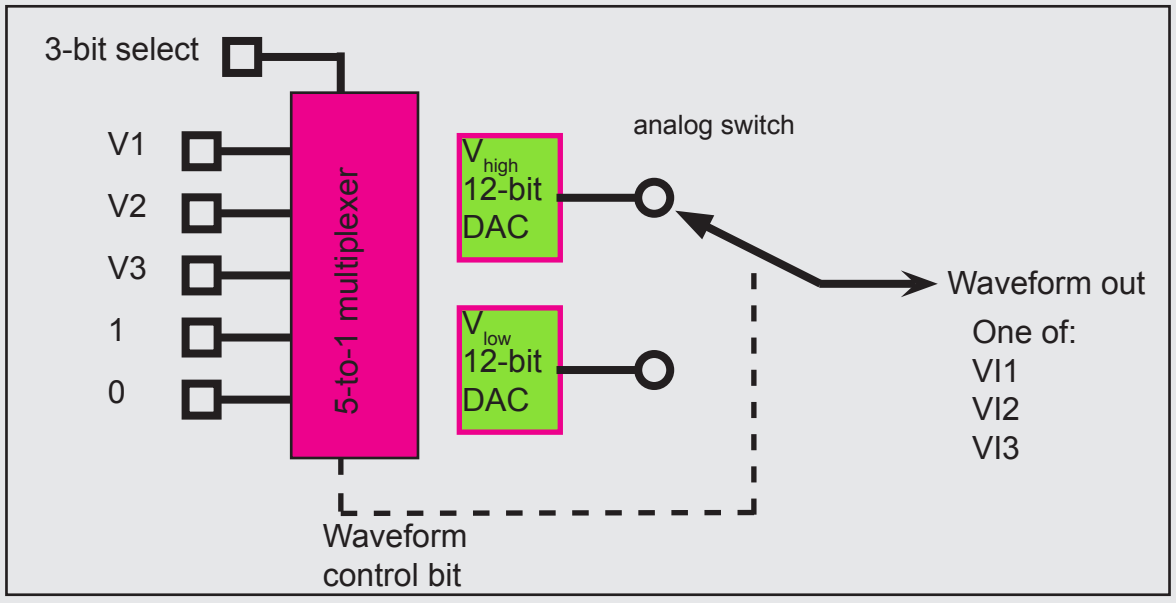


Figure 43. Each of the three VIx (x=1,2,3) output pins has a circuit similar to this one which selects one of the Vx waveform table bits as the control for that output pin.

The values for the parallel clock multiplexer selection bits is shown in Table 17.

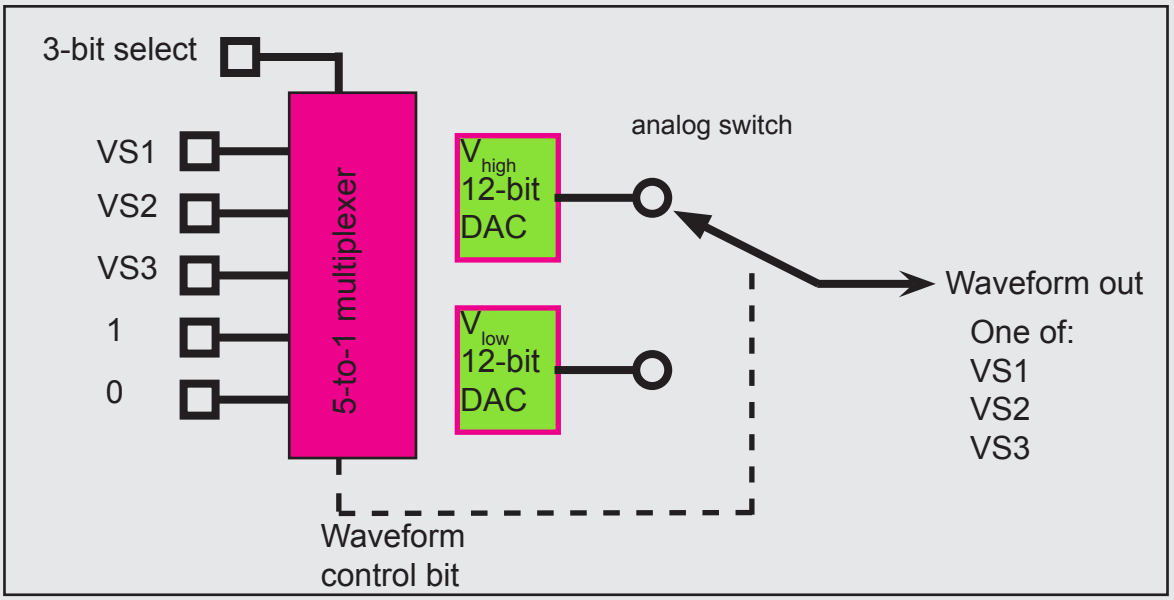


Figure 44. Each of the three VSx (x=1,2,3) output pins has a circuit similar to this one which selects one of the VSx waveform table bits as the control for that output pin.

selection value	VIx input bit selected	VSx input bit selected
1	VI1	VS1
2	VI2	VS2
3	VI33	VS3
4	1	1
5	0	0

Table 17. Selection values for the parallel clocks.

13.1. Waveform tables

The UCAM controller Xilinx steps through the data bytes of the waveform is a strictly linear fashion. It does not have the ability to loop through portions of a waveform. This design has consequences for CCD binning where a portion of the serial or parallel waveform is repeated more than once. To achieve binning the repeated portion of the waveform must be duplicated the appropriate number of times in the waveform. This implies that there are separate waveforms for each desired binning, with the appropriate section of the waveform duplicated to achieve the binning function. Since the memory available to store waveforms is not infinite there must be a limited number of available binning options. The UCAM controller does not support arbitrary binning. In fact we typically support binning by 1, 2, 4, and 8 only.

13.1.1. Serial waveform tables

For the serial clocks there are six distinct waveforms. There are four waveforms for the four binning options, there is a waveform to define the static state of the serials when they are not clocking, and there is a waveform for skipping over unwanted pixels. Each of the six waveforms is stored in memory with a unique, fixed memory starting address. For the serial clocks there is always a pairing of one byte for the actual serial clocks and one byte for the video processing. So there is actually a pair of

addresses for each of the six waveforms. Those serial waveform starting addresses are shown in Table 18.

Usual label	Serial clocks waveform address (hex)	Video processing waveform address (hex)	Description
bin1	8000	a000	Serial binning X1
bin2	8100	a100	Binning X2
bin4	8200	a200	Binning X4
bin8	8300	a300	Binning X8
hstc	9000	b000	Static serial state
hskip	9100	b100	Pixel skipping

Table 18. Serial waveform table starting memory addresses.

The two serial clocking waveforms are traditionally stored in two separate files, by convention named **clkh1** and **clkh2** for the serial waveform and the video processing waveform respectively. Slight variations on these names are sometimes used, but even those names usually include **clkh1** and **clkh2** in their names.

In order to use the symbolic names as described the first column of Table 13 and Table 14 the serial waveform files are defined using an assembly language syntax. Practically any assembly language could be used since all we are doing is defining a series of constants at fixed memory locations. No actually assembly language instructions are involved. Simply because it is conveniently available we use a 6502 MPU assembler called **as65**. Figure 45 shows side-by-side the headers for the **clkh1** (serial waveforms) and **clkh2** (video processing waveform). The first line in each file is a comment. All comments begin with the semicolon (;). The next eight lines define the basic symbolic names for the values associated with each clock waveform. All of the remaining lines define symbolic names for various combinations of eight basic clocks. These symbolic names will then be used to create the actual waveform tables.

Figure 46 shows the portion of the two files that define the waveforms for serial binning 1X (no binning). Note that the two files look identical. The symbolic names are identical in each file and this helps greatly in assuring that for every byte in the serial clock file there is a matching byte in the video processing file. The details are hidden in the definitions of the symbolic names, as given in the header portion of the file, Figure 45. Note the starting addresses, given by the **.org** line at the beginning of the waveform definitions. These match the values shown in Table 18.

```
;waveforms for H clocks----H1
h1      .equ 1
h2      .equ 2
h3      .equ 4
reset   .equ 8
hwell   .equ 10
nouse1   .equ 20
nouse2   .equ 40
nouse3   .equ 80
;
step1   .equ h2+h3+hwell
step2   .equ h3+hwell
step3   .equ h3+h1+hwell
step4   .equ h1+hwell
step5   .equ h1+h2+hwell
step6   .equ h2+hwell
dtep1   .equ step1
dtep2   .equ step2
dtep3   .equ step3
dtep4   .equ step4
dtep5   .equ step5
dtep6   .equ step6
btep1   .equ step1
btep2   .equ step2
btep3   .equ step3
btep4   .equ step4
btep5   .equ step5
btep6   .equ step6
skp01   .equ step1+reset
skp02   .equ step2+reset
skp03   .equ step3+reset
skp04   .equ step4+reset
skp05   .equ step5+reset
skp06   .equ step6+reset
sgep0   .equ h1+h2+hwell
sbase   .equ hwell+h1+h2
sbase1  .equ hwell+h1+h2
sgep1   .equ h2+hwell
sgep2   .equ h2
;sgep3   .equ h2+hwell
;sdata   .equ h2+hwell
;sdata1  .equ h2+hwell
sgep3   .equ h2
sdata   .equ h2
sdata1  .equ h2
adc1    .equ h2+reset+hwell    ;changed add hwell
adc2    .equ reset+h2+hwell    ;changed add hwell
rst1    .equ reset+h2+h3+hwell
waitf   .equ h2+h3+hwell
wskp0   .equ h2+h3+reset+hwell
```

```
;waveforms for signal processing----H2
clamp   .equ 1          ;IN-reset
sample  .equ 2
pol     .equ 4          ;pol
pol_    .equ 8          ;pol_
dcrs    .equ 10         ;DC restore
stadc   .equ 20                 ;start adc
stsam   .equ 40                 ;start clamp and sample
onep    .equ 80
;
step1   .equ pol
step2   .equ pol
step3   .equ pol
step4   .equ pol
step5   .equ pol
step6   .equ pol
dtep1   .equ pol+dcrs
dtep2   .equ pol+dcrs
dtep3   .equ pol+dcrs
dtep4   .equ pol+dcrs
dtep5   .equ pol+dcrs
dtep6   .equ pol+dcrs
btep1   .equ pol+dcrs+clamp
btep2   .equ pol+dcrs+clamp
btep3   .equ pol+dcrs+clamp
btep4   .equ pol+dcrs+clamp
btep5   .equ pol+dcrs+clamp
btep6   .equ pol+dcrs+clamp
skp01   .equ pol+dcrs+clamp
skp02   .equ pol+dcrs+clamp
skp03   .equ pol+dcrs+clamp
skp04   .equ pol+dcrs+clamp
skp05   .equ pol+dcrs+clamp
skp06   .equ pol+dcrs+clamp
sgep0   .equ pol
sbase   .equ pol+sample+stsam
sbase1  .equ pol+sample
sgep1   .equ pol
sgep2   .equ pol_
sgep3   .equ pol_
sdata   .equ pol_+sample+stsam
sdata1  .equ pol_+sample
adc1    .equ pol_+stadc+dcrs
adc2    .equ pol+dcrs
rst1    .equ pol+clamp+dcrs
waitf   .equ pol+onep+clamp+dcrs
wskp0   .equ pol+onep+clamp+dcrs
;
;
```

Figure 45. The headers of typical serial clocking *and* video processing *waveform table files.*

```
      .org 08000      ; bin 1 (clamp+sample)
bin1  .byte btep1
      .byte btep1
      .byte btep1
      .byte btep2
      .byte btep3
      .byte btep4
      .byte btep5
      .byte sgep0
      .byte sbase
      .byte sbase1
      .byte sgep1     ;h1 to well
      .byte sgep2
      .byte sgep3
      .byte sgep3
      .byte sdata
      .byte sdata1
      .byte sgep3
      .byte adc1
      .byte rst1
      .byte waitf
      .byte waitf
```

```
      .org 0a000      ; bin 1 (clamp+sample)
bin1  .byte btep1
      .byte btep1
      .byte btep1
      .byte btep2
      .byte btep3
      .byte btep4
      .byte btep5
      .byte sgep0
      .byte sbase
      .byte sbase1
      .byte sgep1     ;h1 to well
      .byte sgep2
      .byte sgep3
      .byte sgep3
      .byte sdata
      .byte sdata1
      .byte sgep3
      .byte adc1
      .byte rst1
      .byte waitf
      .byte waitf
```

Figure 46. The typical bin 1X portion of the serial clocking *and* video processing *waveform table files.*

We can use the **wplot** command to interpret the waveform files and to produce a plot of the resulting waveform. (The command in this case would be **wplot clkh1 clkh2**.) The resulting plot is shown in Figure 47. Note that this plot does not show the actual output voltage levels of the clocks. At this point we are only defining the sequence of changes in the data bits at the lowest level. The physical output voltages are created when these bits are routed through the switching circuits of Figure 42.

Additional sections of **clkh1** and **clkh2** define binning X2, X4, X8, and the other waveforms listed in Table 18. Figure 48 shows the bin X2 section of the files with the repeated clocks highlighted in the **clkh1** portion and Figure 49 shows the resulting plot of the waveforms.

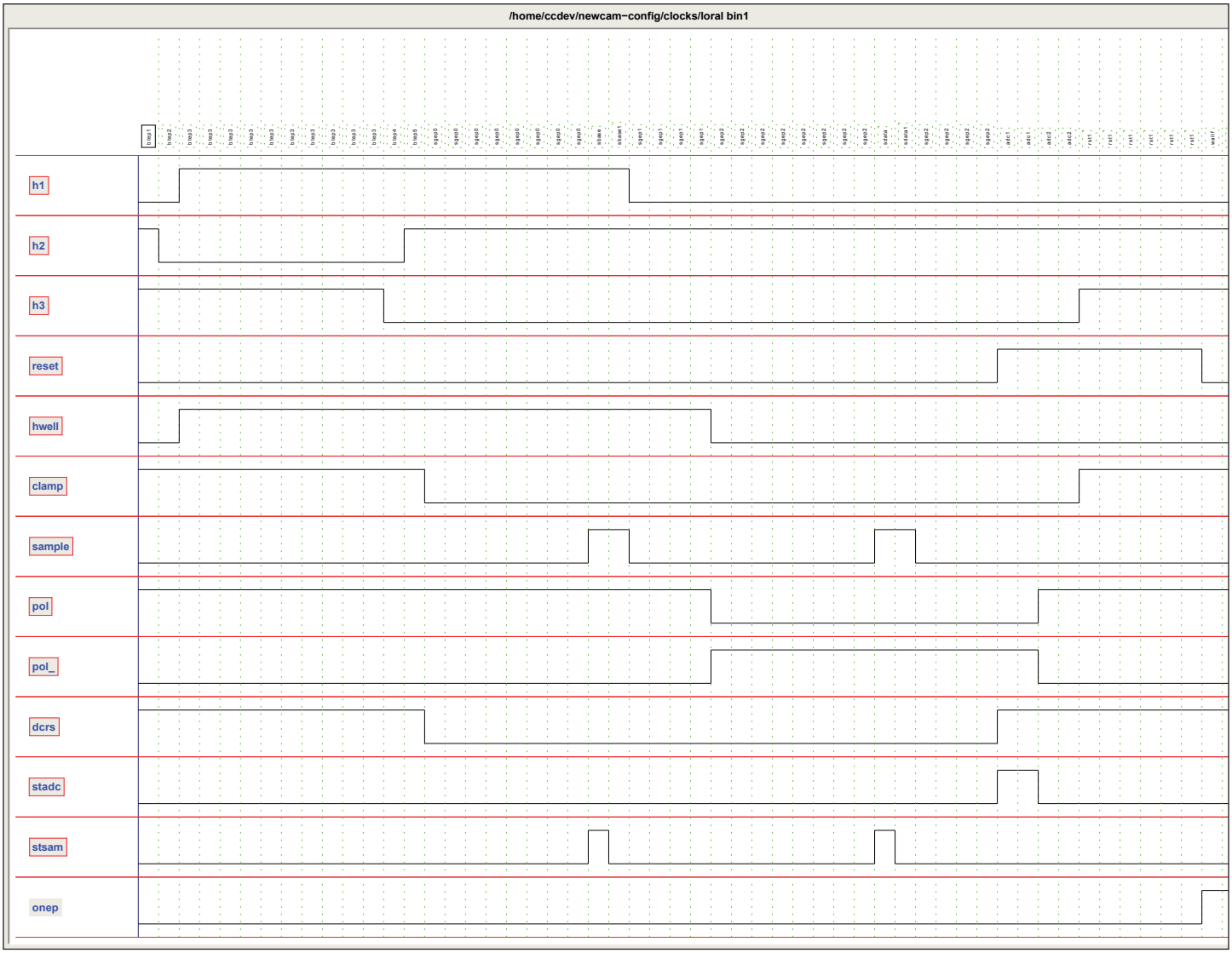


Figure 47. A plot of the bin 1X waveform defined in the sample file.

```
      .org  08100      ; bin 2 (clamp+sample)
bin2    .byte btep1
      .byte btep1
      .byte btep1
      .byte btep2
      .byte btep3
      .byte btep4
      .byte btep5
      .byte btep6
      .byte btep1
      .byte btep2
      .byte btep3
      .byte btep4
      .byte btep5
      .byte sgep0
      .byte sbase
      .byte sbase1
      .byte sgep1     ;h1 to well
      .byte sgep2
      .byte sgep3
      .byte sdata
      .byte sdata1
      .byte sgep3
      .byte adc1
      .byte adc2
      .byte rst1
      .byte rst1
      .byte waitf
      .byte waitf
```

```
      .org  0a100      ; bin 2 (clamp+sample)
bin2    .byte btep1
      .byte btep1
      .byte btep1
      .byte btep2
      .byte btep3
      .byte btep4
      .byte btep5
      .byte btep6
      .byte btep1
      .byte btep2
      .byte btep3
      .byte btep4
      .byte btep5
      .byte sgep0
      .byte sbase
      .byte sbase1
      .byte sgep1     ;h1 to well
      .byte sgep2
      .byte sgep3
      .byte sdata
      .byte sdata1
      .byte sgep3
      .byte adc1
      .byte adc2
      .byte rst1
      .byte rst1
      .byte waitf
      .byte waitf
```

Figure 48. The typical bin 2X portion of the serial clocking and video processing waveform table files.

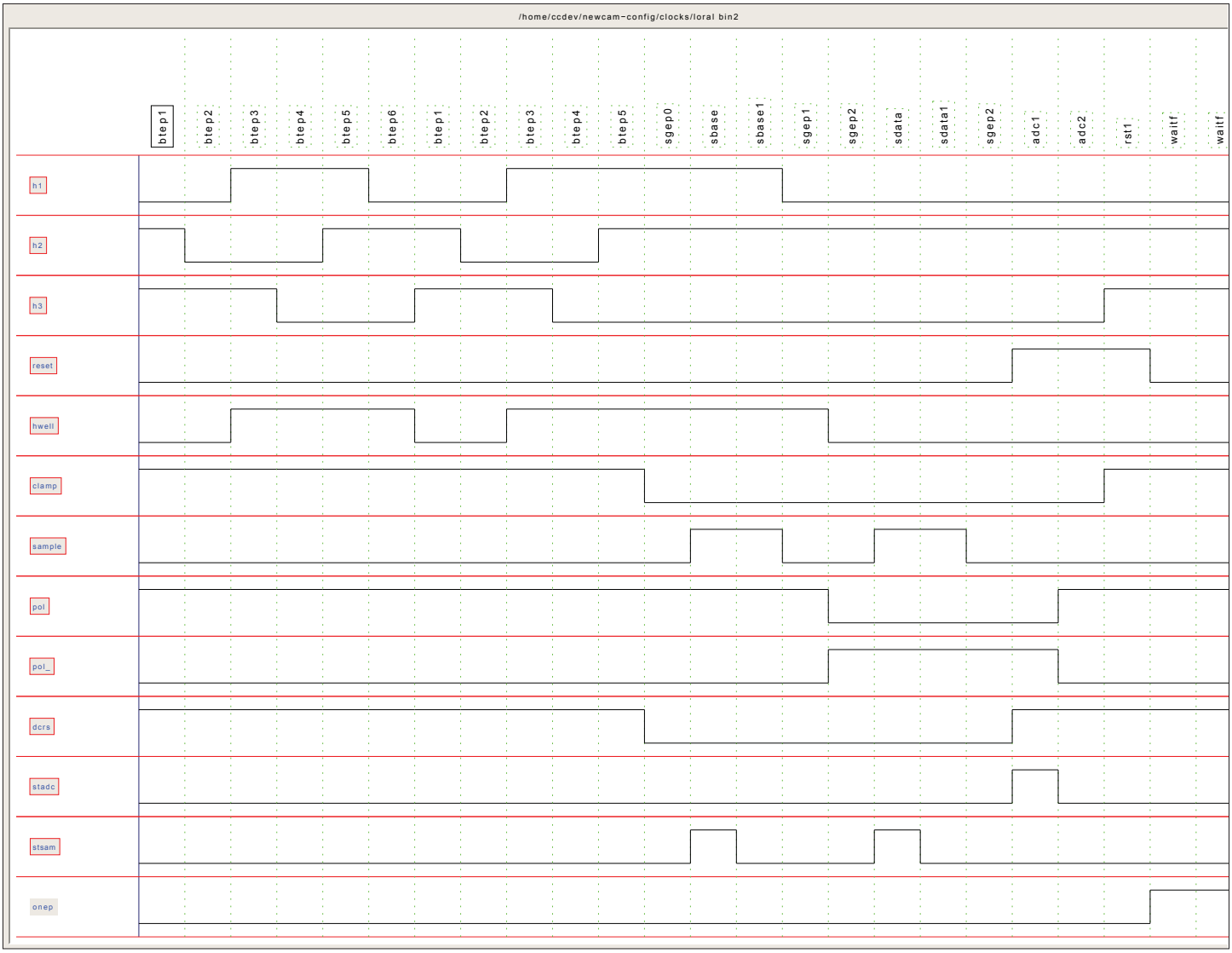


Figure 49. A plot of the bin 2X waveform defined in the sample file.

13.1.2. Parallel waveform tables

The parallel clocks are typically stored in a file called **clkv**. The structure is the same as the serial clock files, with a header defining a set of symbolic names and a set of waveforms produced using the symbols. As with the serial clocks there are variety of waveforms defined to produce the desired parallel clocking patterns. There are separate waveforms for parallel binning 1X, 2X, 4X, and 8X. Also, to accommodate leaving the parallel clocks in the MPP state all of the binning waveforms have both an MPP version and a non-MPP version. The starting addresses for all of the different parallel clock waveforms are detailed in Table 19.

Usual label	Parallel clock waveform addresses (hex)	Description
framet	c000	Frame transfer non-mpp
static	c100	Static for special baseline readout
ersp	c200	mpp up bin1 special erase
sndb1	c300	non-mpp down bin 1X
snub1	c800	non-mpp up bin 1X
snub2	c900	non-mpp up bin 2X
snub4	ca00	non-mpp up bin 4X
snub8	cb00	non-mpp up bin 8X
mstatic	d100	all low for mpp
smdb1	d300	mpp down bin 1X
smub1	d800	mpp up bin 1X
smub2	d900	mpp up bin 2X
smub4	da00	mpp up bin 4X
smub8	db00	mpp up bin 8X

Table 19. Parallel waveform clock starting memory addresses.

13.1.3. Waveform files

Waveform tables are by convention stored in the directory **/home/ccdev/newcam-config/clocks**. Within the **clocks** directory are a set of subdirectories, one for each type of CCD for which waveform tables have been defined. The waveform table files are stored in these subdirectories. The examples shown in this document have come from the **loral** subdirectory. Also by convention the official version of the files are stored on the machine **pixel** in the CCD Development Lab. Other machines have copies of the files stored on **pixel**. If changes are made to waveform files on other machines those changes need to be copied back to **pixel**. (It would be good to place all of the waveform files under **cvs** management. This is a task for the future.)

In the subdirectories where the waveform table files are stored there is usually a script file called **how**. This script encapsulates all of the commands needed to assemble the waveform files with **as65** and turn the output from the assembler into a file that can be downloaded to the controller.

13.2. Mapping waveforms to output pins

The mapping of waveforms to output pins is essentially invisible to the user. Figure 42, Figure 43, and Figure 44 each specify a 3-bit waveform selection value that controls the multiplexer. The user never writes these values directly. Instead the user sends commands to the UCAM controller to tell it how to operate the CCD and the TIM board CPU figures out the three sets of multiplexer control values needed to produce the requested operating mode.

13.3. Waveform timing

The reader may have noticed that we have not mentioned waveform timing until now. That is because the waveforms do not specify time in absolute units. Each entry in a waveform table will last for a fixed period of time, T_W. After a time T_W the next waveform entry is output. This continues until the last entry in the waveform table ends the sequence. The value of T_W, in microseconds for instance, is not specified in the waveform. Instead, there are separate commands which can be sent to the controller that specify the value T_W. In fact there are two values, T_{WS} and T_{WP} which define the serial and parallel clock timing independently.

13.4. Downloading waveforms to UCAM controller

The easiest way to download new waveforms to the UCAM controller is to use the facilities provided in the Lick data acquisition software. In the main gui of that software there is an *Engineering* tab (abbreviated *Eng.*). Select that tab. In the engineering window select *Download*. A new window pops up which allows you to select a file. Click the *Select File* button and navigate to the desired waveform binary file (they end in the suffix **.bi**). Select the file and click the *Open* button. Now all you have to do is click the *Dowload Obj File* button and the file is transmitted to the controller.

14. Setting Up a New Controller

In this section we describe how to assemble and setup up a new controller.

14.1. Voltage Calibrations

14.1.1. Bias voltages

14.1.2. Clock voltages

14.1.3. Main power supplies

14.1.4. TCB power supplies

14.2. Temperature Calibrations

14.2.1. Dewar temperature

14.2.2. Room temperature

14.2.3. Temperature display meter

14.3. How to create a voltage file (file format) and setup voltages

How to change voltages

14.4. How to create a clock file and download it

14.5. How to add a new camera(CCD) to the UCAM

14.5.1. change ID file (ID file format?)

14.5.2. download waveforms

14.5.3. download voltages

14.6. How to configure (initial) a new controller:

14.6.1. old CDB board or new CDB board

14.6.2. old SPB board or new DSPB board

14.6.3. old ADC board or new QADC board

14.7. SEEPROM in preamp box work?

(ID=FFH)

14.7.1. How to save parameters to the SEEPROM (>WI)

14.7.2. How to recover a system from a SEEPROM (>RA)

14.7.3. How to save parameters to the P memory (>SP)

14.7.4. How to save clocks to the C memories (>SC)

15. Appendix A - Hardware Specification Registers

15.1. Addresses

Beginning with TIM software version 4.02 the following TIM memory addresses provide information about the hardware configuration.

Address	Meaning	
0bf0	0 ≥ 2	Two old SPBs Number of DSPBs
0bf1	0 ≥1	Old CDB Number of new CDBs
0bf2	0 ≥1	Old 2-channel ADC Number of 4-channel ADC boards (QADC)
0bf3	0 1	Old timing board New timing board

Table 20. Hardware Configuration registers stored in the TIM.

Video channels are routed to ADCs via analog switches. The ADCs are then read and transmitted over the fiber optic cable. Associated with each ADC is a memory location that indicates which video channel is connected to that ADC. The memory locations are show in the following table for one QADC (0bf2 =1).

08c0	First ADC transmitted
08c1	Second ADC transmitted
08c2	Third ADC transmitted
08c3	Fourth ADC transmitted

Table 21. TIM memory locations that define the association of video channels and ADCs.

The value stored at the addresses show in Table 20 indicates which video channel is connected to that ADC. The values for a 4-amplifier CCD are show in the following table.

0	a0/AR
1	b0/BR
2	b1/BL
3	a1/AL

Table 22. Legal values for the video-to-ADC mapping locations described in Table 20.

16. Appendix B - UCAM Backplane Pin Assignments

#	A	B	C
1	-5V A	+5V A	
2	-15V A	+15V A	+15V A
3			AD0
4	MOSI		AD1
5	MISO		AD2
6	SCLK		AD3
7			AD4
8	RESET		AD5
9	GND		GND
10	DONE2		AD6
11	GND		AD7
12	20MHZ	CLAMP_	ALE
13	RID	SAMPLE_	AA0
14		DCR_	AA1
15	GND	POL	AA2
16	RD_	POL_	AA3
17	GND	FI-VI1	FI-H1
18		FI-VI2	FI-H2R
19	GND	FI-VI3	FI-H3R
20		GND	FI-W
21		FI-TB	FI-H2L
22		FI-VS1	FI-H3L
23	WCDB	GND	FI-R
24	WSPB0	FI-VS2	FI-HSPR
25	WSPB1	FI-VS3	LDPAR
26	AADCB	FI-TA	LPDONE
27	WTESTB	SHUTTER	ADCCLKIN
28	RTESTB	V-TEST	
29	WR_	INRDCCD	TV-SPR
30	VSEL_	GND-light	T-BIAS
31			
32	VCC	VCC	VCC

Table 23. The UCAM backplane pin assignments.

Index

Symbols

B

C

D

E

F

G

H

I

J

O

P

R

S

T

U

W

X