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CCD42-90 Back Illuminated Deep Depletion 2048 x 4608 pixel Scientific CCD Sensor

FEATURES

- 2048 x 4608 x 13.5 µm pixels
- Back Illuminated Operation - High QE
- Low Noise Output Amplifiers
- 3-Side Buttable Package
- 100% Active Area
- Flatness better than 15 µm peak-to-valley
- Gated Dump Drain on Output Register
- Optimised for Increased Red Response

INTRODUCTION

This version of the CCD42 family of CCD Sensors has full frame architecture. Back illumination technology, in combination with an extremely low noise amplifier, make the device well suited to the most demanding applications such as astronomy. This variant is manufactured in high resistivity silicon of increased depth, which gives exceptional red wavelength sensitivity.

The output amplifier is designed to give excellent noise levels at low pixel rates and can match the noise performance of most conventional science CCDs at pixel rates as high as 1 MHz. The low output impedance of approx. 350 Ω simplifies the interface with external electronics, and a resistor and U309 JFET are also included in the package for each amplifier to give the option of an additional source follower buffer stage.

The readout register has a gate controlled dump drain to allow fast dumping of unwanted data. The register is designed to accommodate 4 image pixels of charge and a summing well is provided capable of holding 6 image pixels. The output amplifier has a feature (switchable OG2 gate) to enable the responsivity to be reduced to allow the reading of such large charge packets.

The device is supplied in a package designed to facilitate the construction of large close-butted mosaics and is designed to be used cryogenically. The design of the package will ensure that the flatness is maintained at the working temperature.

The device is shipped in a protective container, but no permanent window is fitted.

This short-form data sheet details the performance of the deep depleted versions of CCD42-90. Refer to the full CCD42-90 Back Illuminated data sheet for more detailed information on driving the device and for interface details.

GENERAL DATA

Format

Image area	27.6 x 62.2 mm
Active pixels:	
horizontal.....	2048
vertical.....	4608 + 4
Pixel size	13.5 x 13.5 µm

50 additional pixels are provided for overscanning purposes.

Number of output amplifiers..... 2

The device has a 100% fill factor for maximum sensitivity.

PACKAGE

Format	metal pack with 40-pin PGA connector
Size	28.2 x 67.3 mm
Focal plane height, above base (shim pads)	14.0 mm
Inactive edge spacing (nominal; 50 µm tolerance)	
sides.....	260 µm
top.....	120 µm
bottom (edge connections)	5.0 mm

TYPICAL PERFORMANCE

Output amplifier responsivity	4.5 µm/e ⁻
Peak signal.....	150,000 e ⁻ /pixel
Register charge capacity.....	600,000 e ⁻ /pixel
Summing well charge capacity	900,000 e ⁻
Charge transfer efficiency:	
parallel.....	99.9995%
serial	99.9995%

Quantum Efficiency – See table overleaf

Minimum spectral range	200 – 1100 nm
Readout noise (140 – 230 K).....	3 e ⁻ rms
Dark current (173 K).....	1 e ⁻ /pixel/hr

Note: All values quoted using typical operating conditions at a readout frequency of 20 kHz and at a temperature of 173 K (approx).

Typical Operating Conditions

Ref	Pin No	Typ.Voltage
Vss	A1, A8, C1, C8, F2, F7	9 V
IØ1	D8	10 V
IØ2	E8	10 V
IØ3	F8	10 V
RØ1(L)	D4	11 V
RØ2(L)	E4	11 V
RØ1(R)	D5	11 V
RØ2(R)	E5	11 V
RØ3	F6	11 V
ØR(L)	E3	12 V
ØR(R)	E6	12 V
ØSW(L)	E2	11 V
ØSW(R)	E7	11 V
DG	F3	0 V; see note 3
OG1(L)	D3	3 V
OG1(R)	D6	3 V
DD(L)	B2	24 V
DD(R)	B7	24 V
OG2(L)	D2	see note 1
OG2(R)	D7	see note 1
OD(L)	B1	29 V
OD(R)	B8	29 V
OS(L)	A2	see note 2
OS(R)	A7	see note 2
RD(L)	C2	17 V
RD(R)	C7	17 V

Optional connections for U309 JFET

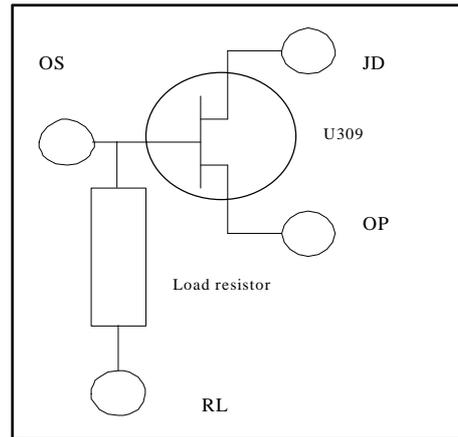
RL (L)	A3	AGND (0 V)
RL(R)	A6	AGND (0 V)
OP (L)	B3	See note 4
OP(R)	B6	See note 4
JD (L)	C3	OD (L) + 2 V
JD(R)	C6	OD(R) + 2 V

- Connections to the package are made by a pin grid array.
- Pins D1, E1, F1 are not connected to the CCD.
- Pins D1, F1 are used for a temperature sensor (some versions).
- Clock pulse low levels = 0 V (± 0.5 V); except RØ low + 1 V.
- The CCD is not electrically connected to the metal package.

Nomenclature

Vss	-	Substrate
AØ1, AØ2, AØ3	-	Image area clocks
RØ 1/2/3	-	Serial register clocks
ØR	-	Reset clock
ØSW	-	Summing well
DG	-	Register dump gate
OG1, OG2	-	Output gates
DD	-	Dump drain
OD	-	Output drain
OS	-	Output source
RD	-	Reset drain
RL	-	Load resistor (for FET use)
OP	-	JFET source (output)
JD	-	JFET drain

Detail of FET buffer



NOTES

1. $OG2 = OG1 + 1$ V = 4 V (typ) - normal low noise mode,
or = 20 V - Low responsivity / increased charge handling mode.
2. $OS = 3$ to 5 V below OD typically. Use 3 - 5 mA current source, or 5 - 10 kΩ load.
3. Non-charge dumping level is shown. For charge dumping DG should be pulsed to 12 ± 2 V.
4. The JFET is floating, with its gate connected to OS. A floating 10 kΩ load resistor is also connected to OS. The FET may be used to buffer the chip output (OS) if desired; in this case, connect FET output to AGND via a 5 mA load, and RL directly to AGND.

BLEMISH SPECIFICATION

Maximum allowed defect levels are indicated below.

Grade	0	1	2	5
Column defects - black or white	6	12	20	NS
White spots	450	800	1500	NS
Traps > 200e ⁻	30	50	80	NS
Total spots (black & white)	1350	2000	3500	NS

NS: Not specified.

Black spots are counted if the response is less than 50% of the local mean.

White spots are counted if they have a generation rate equivalent to 300 e⁻/pixel/min at -100 °C. (This is equivalent to a previously used definition of 100 e⁻/pixel/hr at -120 °C).

Note: This deep-depletion variant has a different cosmetic specification to the standard silicon device.

PERFORMANCE LIMITS (at 173 K unless stated)

Parameter	Min	Typical	Max	Units	Notes
Peak charge storage	100k	150k	-	e ⁻ /pixel	5
Peak output voltage (unbinned)	-	675	-	mV	
Register charge capacity	-	600k	-	e ⁻ /pixel	
Summing well capacity	-	900,000	-	e ⁻	
Dark signal at 153 K	-	0.01	2	e ⁻ /pixel/hr	6
Charge transfer efficiency: parallel	99.999	99.9995	-	%	7
serial	99.999	99.9995	-	%	
Output amplifier responsivity	3.0	4.5	6	μV/e ⁻	
Readout noise at 173 K	-	3.0	5.0	rms e ⁻	8
Readout frequency	-	50	3000	kHz	9
Output node capacity	-	900,000	-	e ⁻	10

NOTES

General – **Grade 5** devices are fully functional devices for setup purposes only. Image quality is below that of grade-3, and all other performance parameters may not be met.

- Signal level at which resolution begins to degrade.
- The typical average (background) dark signal at any temperature T (kelvin) between 150 K and 300 K is given by: $Q_d/Q_{do} = 122T^3e^{-6400/T}$, where Q_{do} is the dark current at 293 K. Note that this is typical performance and some variation may be seen between devices.
- CTE is measured for a complete 3-phase clock triplet.
- Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 10 μs integration period.
- Readout above 3000 kHz can be achieved but performance to the parameters given cannot be guaranteed.
- With output circuit configured in low responsivity/increased charge handling mode.

Part reference:

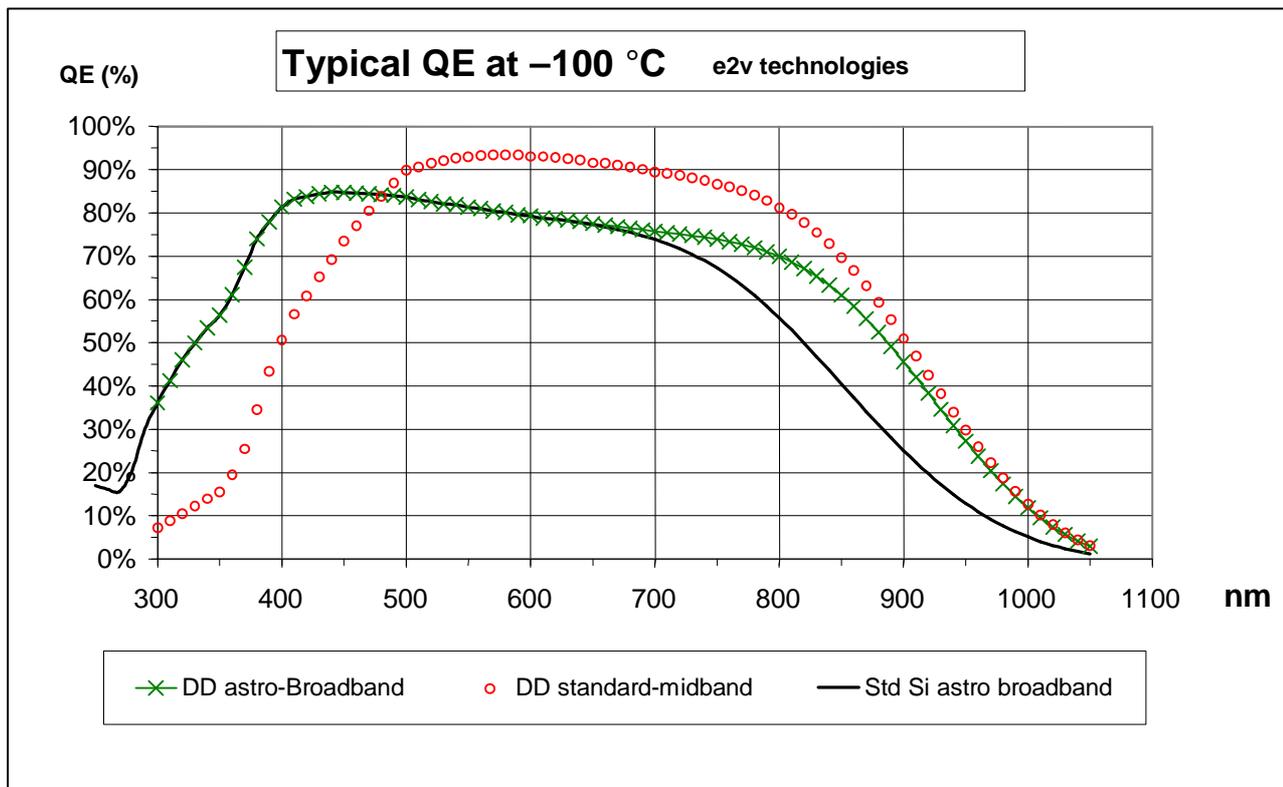
CCD42-90-*-A20 * = grade A20 = variant type: non-IMO, standard process, deep-depletion, midband coating.
 CCD42-90-*-B32 * = grade B32 = variant type: non-IMO, astronomy process, deep-depletion, broadband coating.

SPECTRAL RESPONSE (at 173 K)

Wavelength (nm)	QE (%)		QE (%)		QE (%)	
	Deep depletion silicon		Deep depletion silicon		Standard silicon	
	Min.	Typ.	Min.	Typ.	Min	Typ.
	Standard process Midband coating		Astronomy Process Broadband Coating		Astronomy Process Broadband Coating	
350	10	17	40	50	40	50
400	30	52	70	80	70	80
500	80	92	75	85	80	85
650	85	93	70	80	75	80
900	50	55	45	50	25	30
Device type	CCD42-90-x-A20		CCD42-90-x-B32		CCD42-90-x-B40	

TYPICAL SPECTRAL RESPONSE CURVES

The two primary deep depletion devices are indicated by symbols. For comparison, the standard silicon, astro-broadband response is shown as a solid line. Other variants can be supplied; contact e2v technologies for details.



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